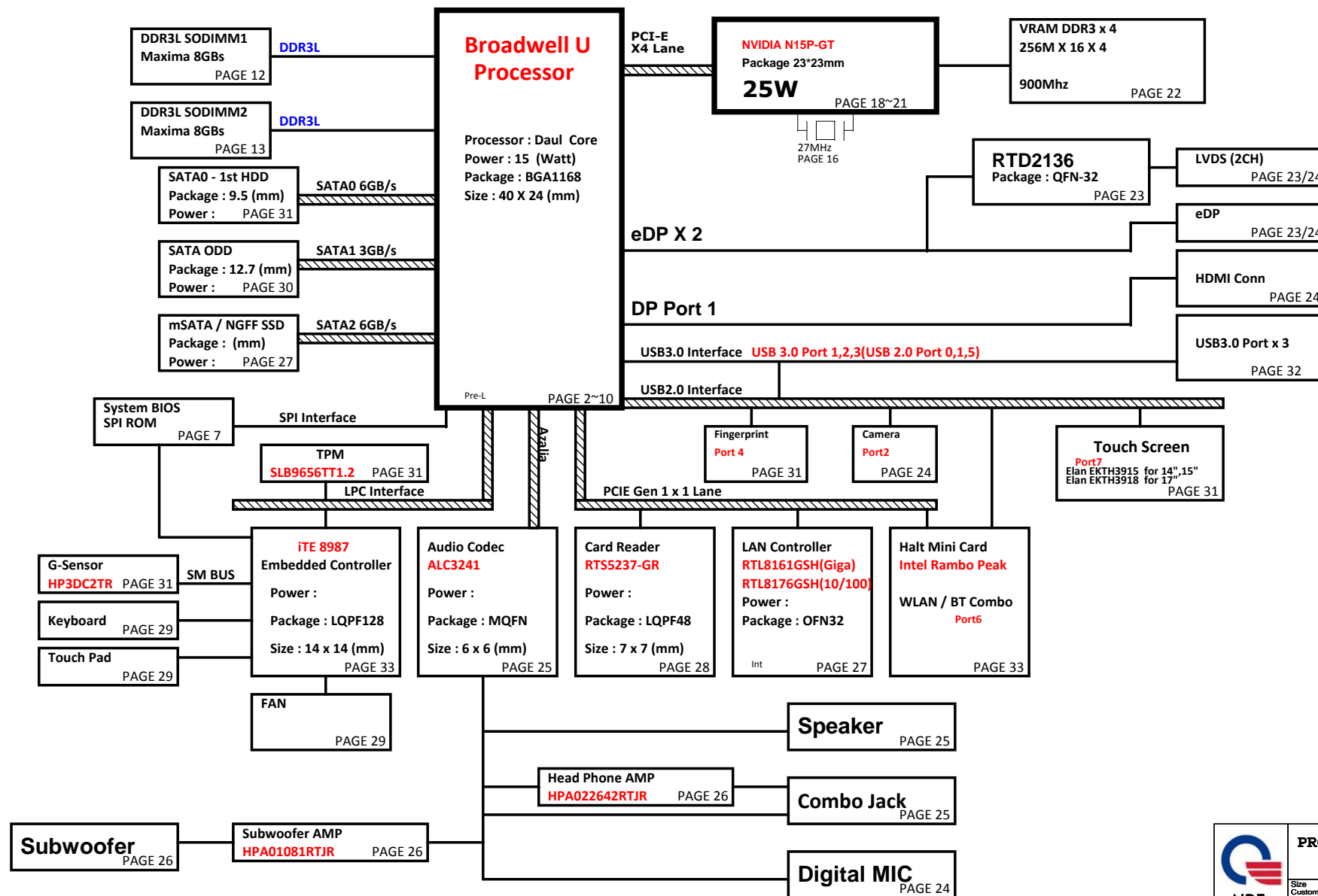


# DIS (14" / 15" / 17") S-Vine<sup>MT</sup> Intel Crescent Bay ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT

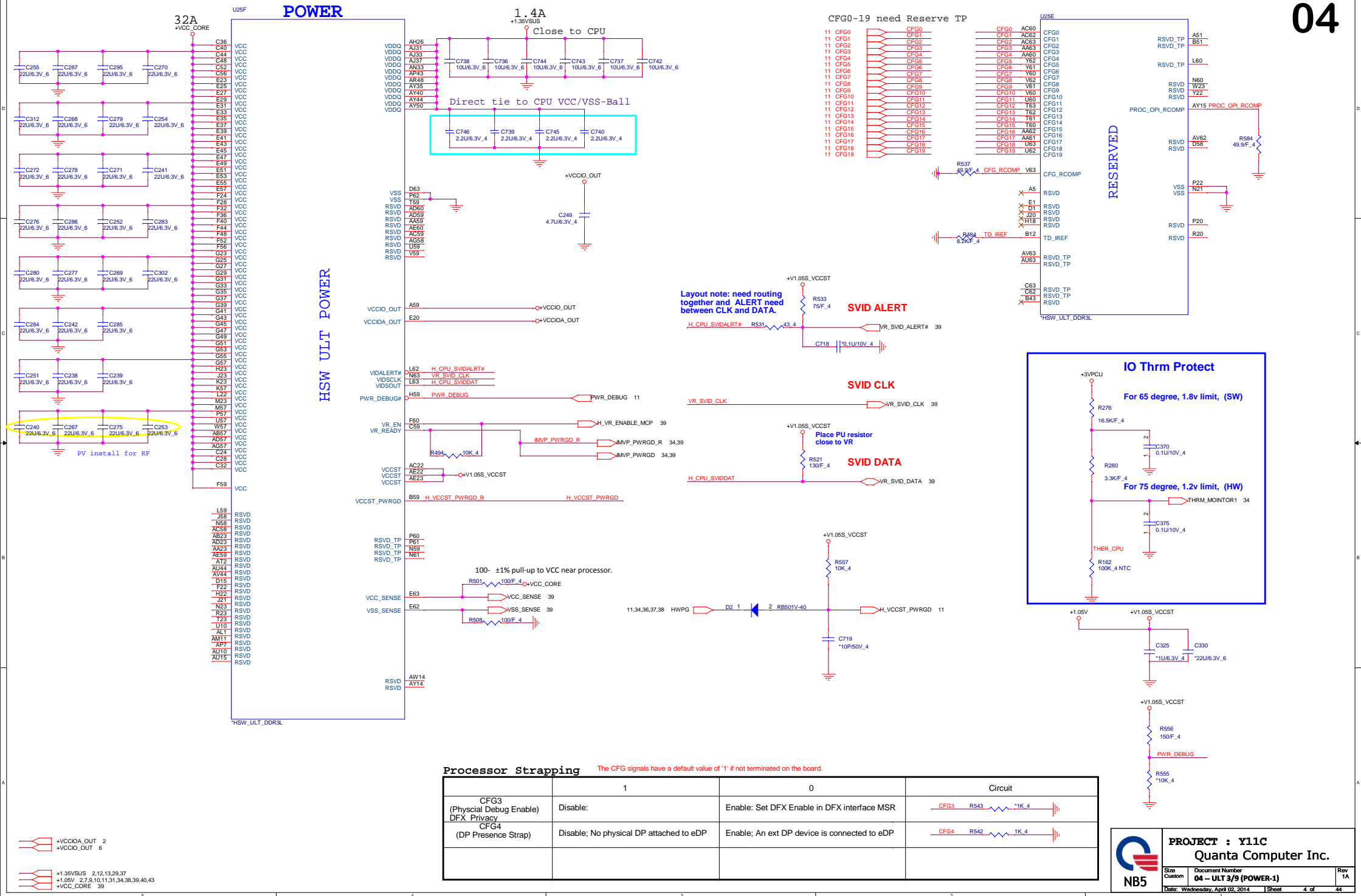


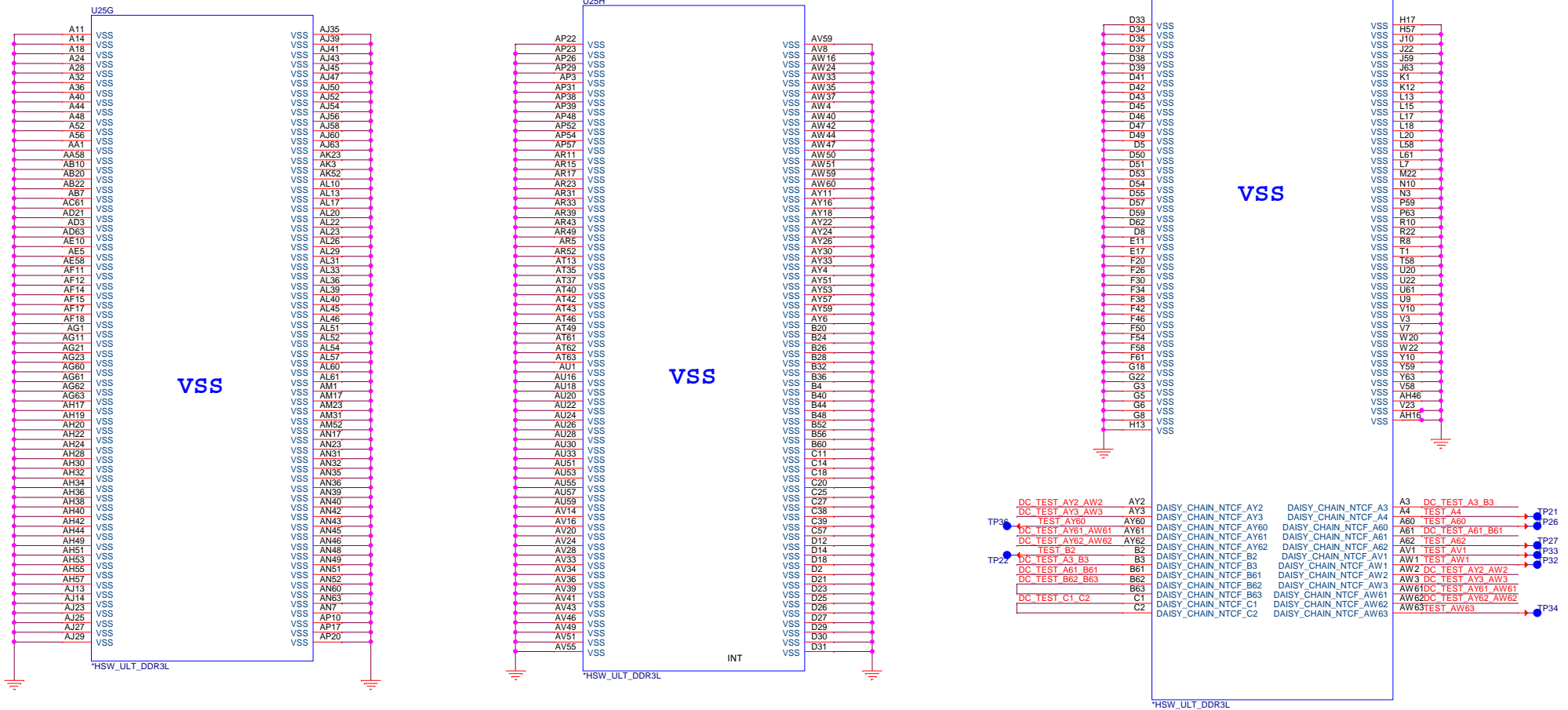


### Processor pull-up (CPU)



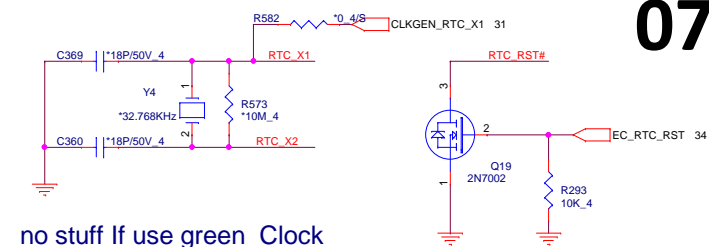
[illegible]





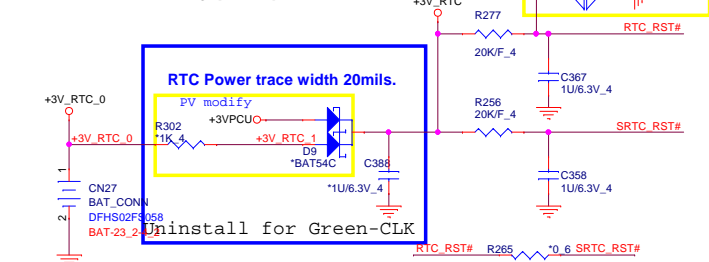


Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTCO—R575—330K 4—PCH_INVRMEN						
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridden	34 GPIO33_EC—R581—1K 4—ACZ_SDOUT						
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"><thead><tr><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>LPC</td></tr><tr><td>0</td><td>SPI(Default)</td></tr></tbody></table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)	
GNT0#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTCO—R576—330K 4—DSWVRMEN 6						
				<div>34 PCH_SPI_CS0#_R—PCH_SPI_CS0#_R</div> <div>34 PCH_SPI1_CLK_R—PCH_SPI1_CLK_R</div> <div>34 PCH_SPI1_SI_R—PCH_SPI1_SI_R</div> <div>34 PCH_SPI1_SO_R—PCH_SPI1_SO_R</div>						

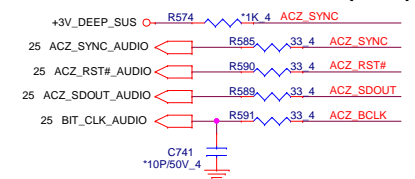


no stuff If use green Clock

### RTC Circuitry(RTC)



## HDA Bus(CLG)

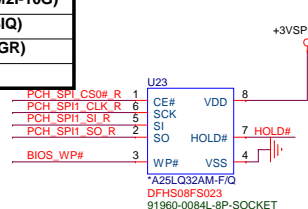


## GPIO Pull UP



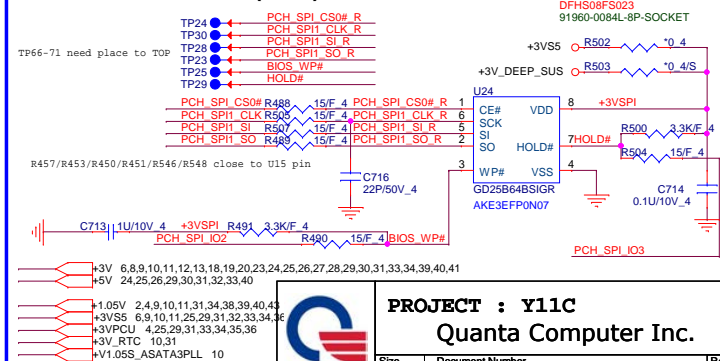
Vender	Size	P/N
MXIC	8MB	AKE3EZLN0Z00 (MX25L6473EM2I-10G)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

### 4M SPI ROM Socket



U10&U15 footprint 要重疊

## PCH SPI ROM(CLG)



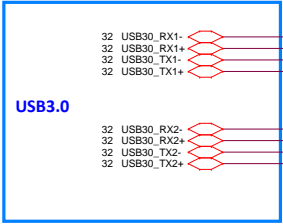
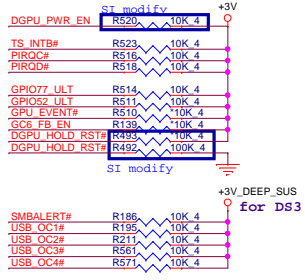
PROJECT : Y11C  
Quanta Computer Inc.

Size Custom	Document Number <b>ULT 6/9(SATA/HDA)</b>	Re
Date: Wednesday, April 02, 2014	Sheet 7 of 44	

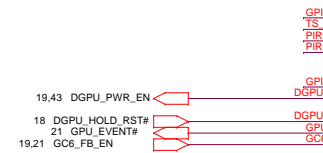


Lynx Point-LP Platform Controller Hub  
(HDA, JTAG, SATA)

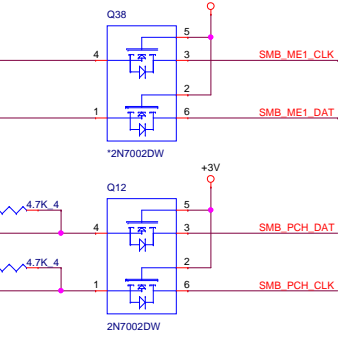
PCI/USBOC# Pull-up(CLG)



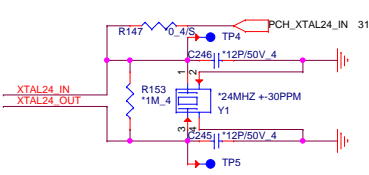
20111130 Modify USB3.0 for HM70



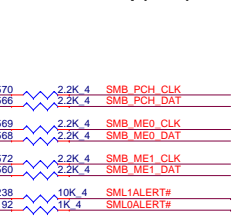
SMBus/Pull-up(CLG)



CLK\_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



PROJECT : Y11C  
Quanta Computer Inc.

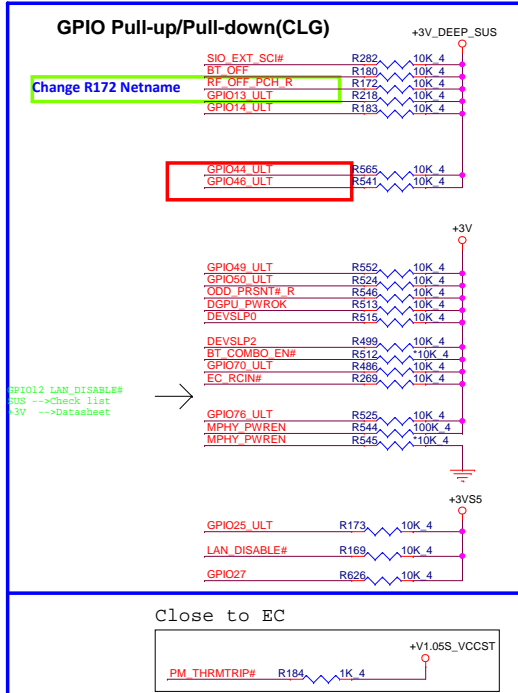
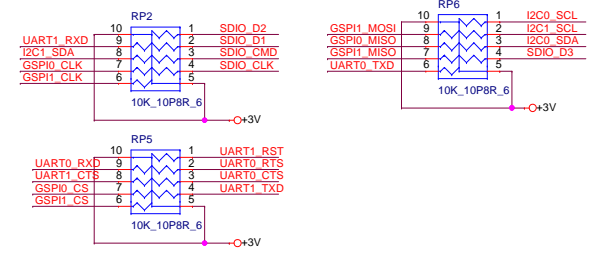
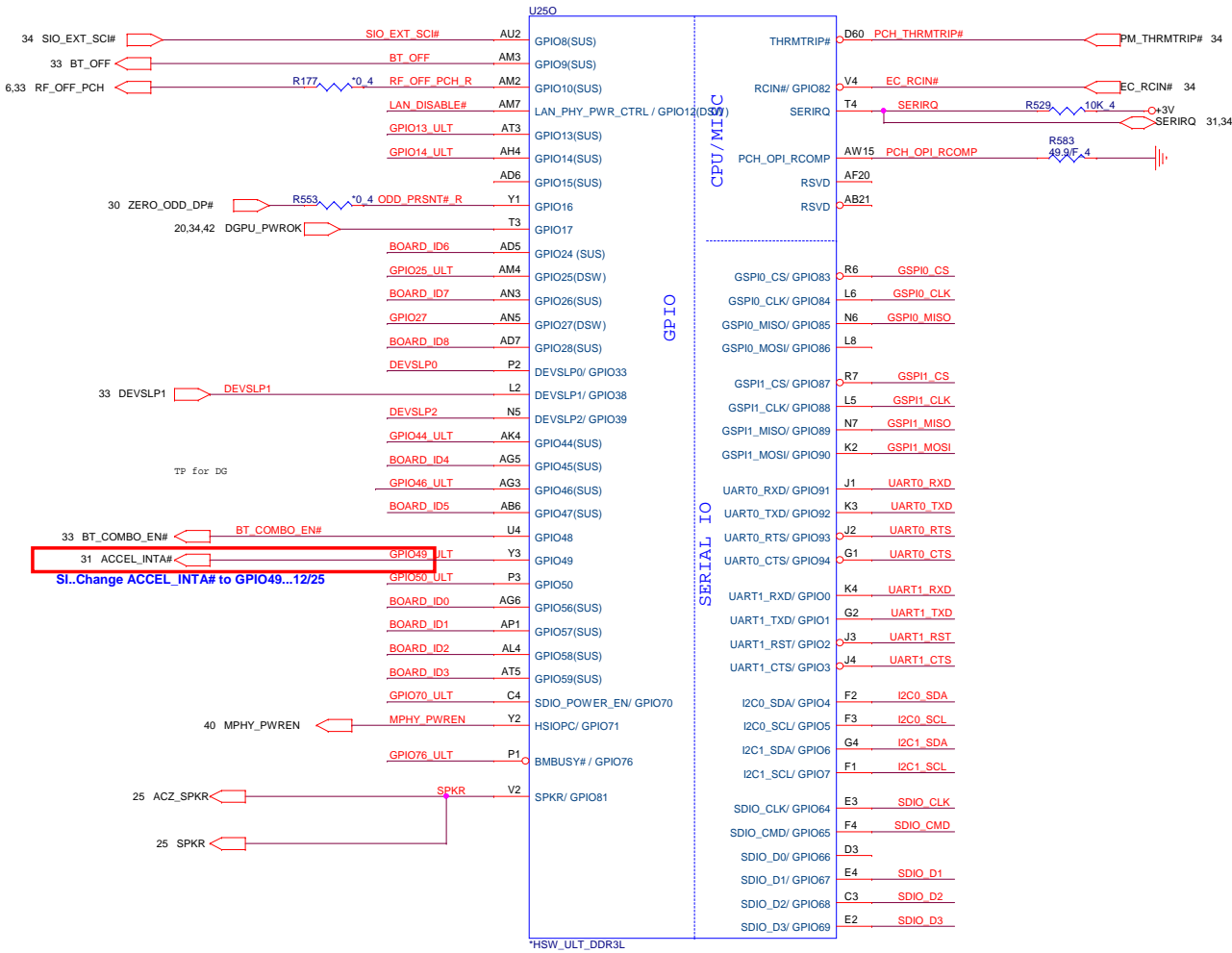
Size Custom  
Document Number  
ULT 7/9 (PCIE/USB/CLK)  
Date: Wednesday, April 02, 2014  
Sheet 8 of 44

NB5

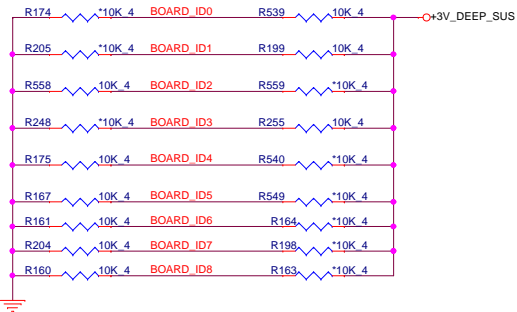


Lynx Point-LP Platform Controller Hub  
(HDA,JTAG,SATA) Haswell (GPIO)

09



Model	BOARD_ID[6:5] Reserve	BOARD_ID4 Reserve	BOARD_ID3 Pavillian 0 1 Envy	BOARD_ID[2:1] 00 14" 01 15" 10 17"	BOARD_ID0 0 : UMA 1 : DIS



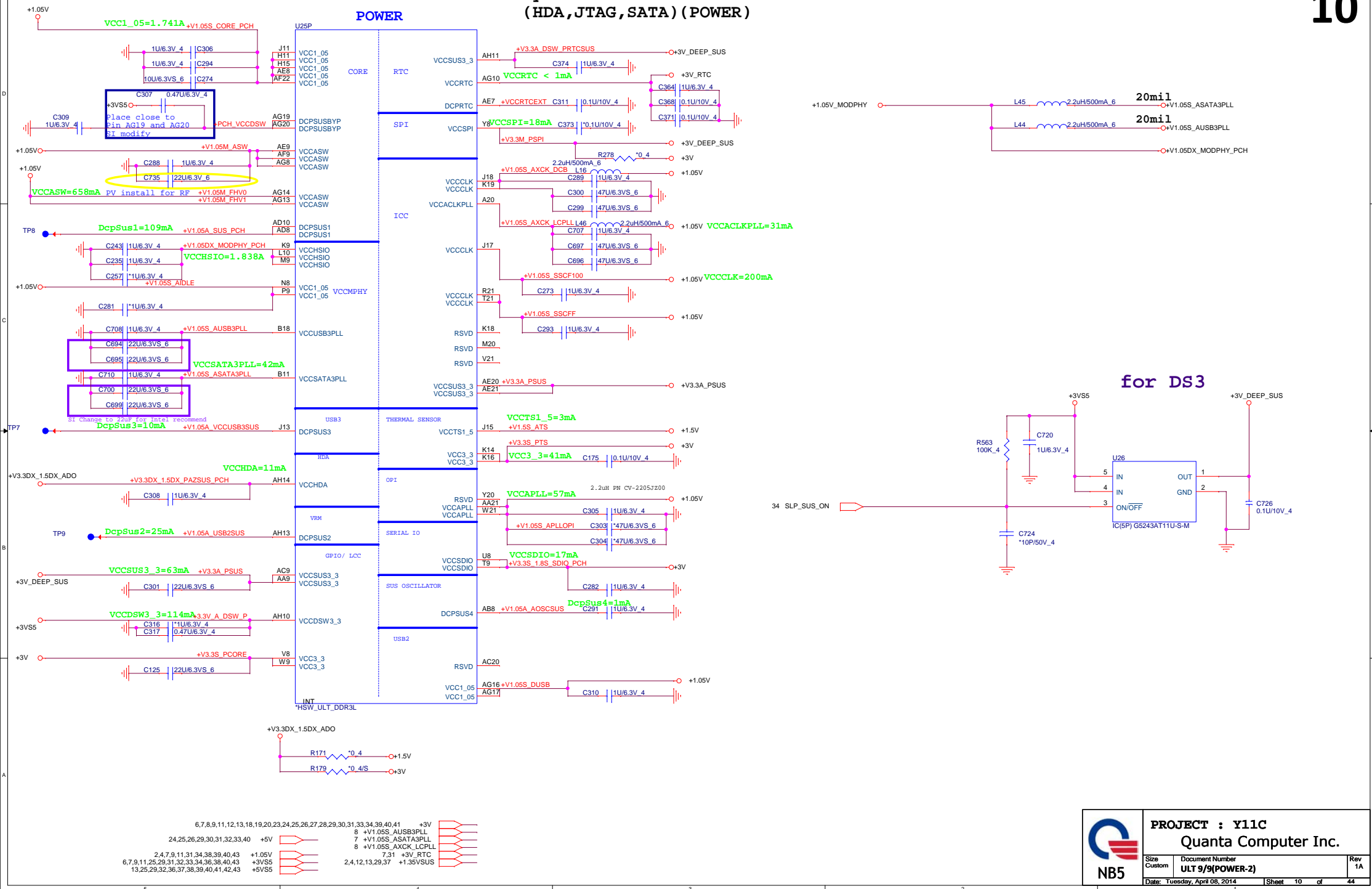
	DIS	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT : Y11C  
Quanta Computer Inc.

Size Custom Document Number ULT 8/9 (GPIO/MISC) Rev 1A

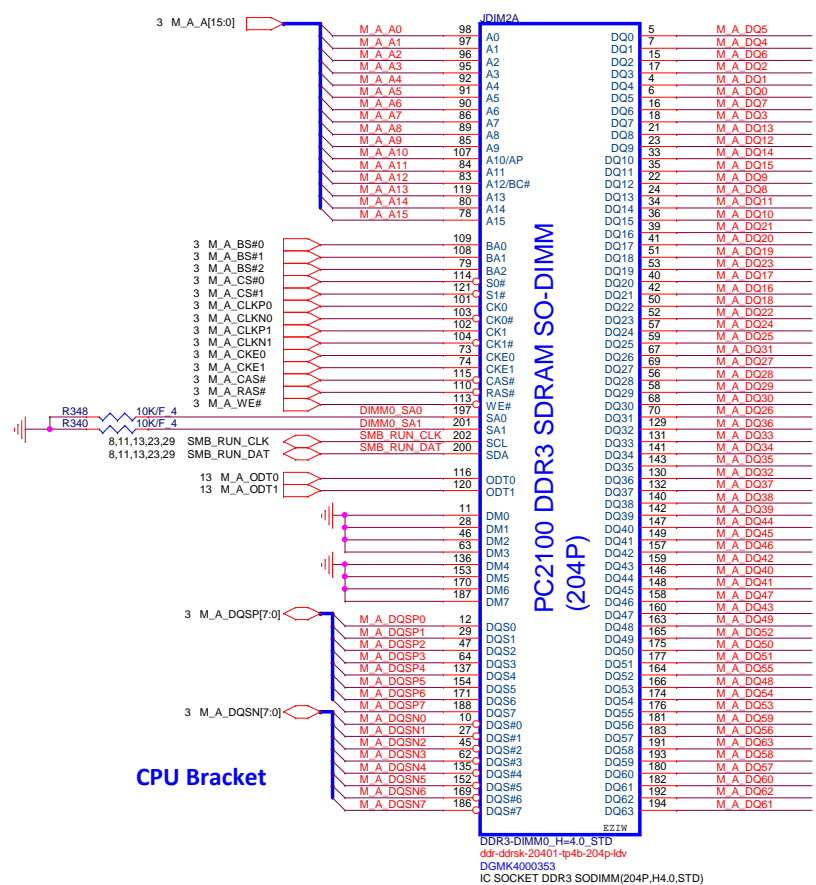
Date: Wednesday, April 02, 2014 Sheet 9 of 44

## Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)(POWER)



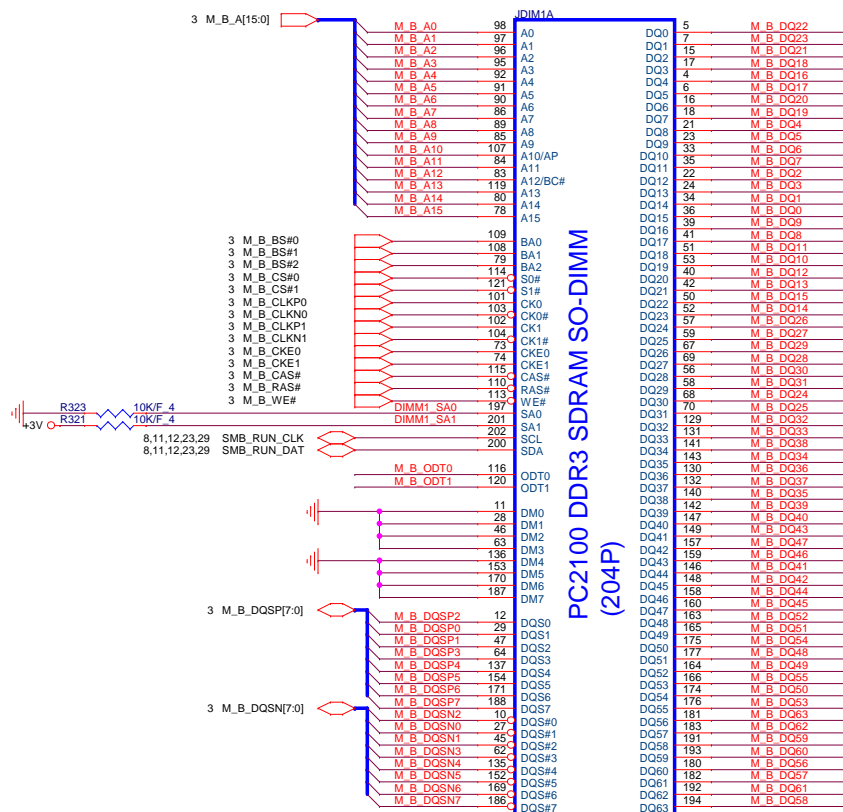


## DIMM &amp; Footprint 同Joshua提供

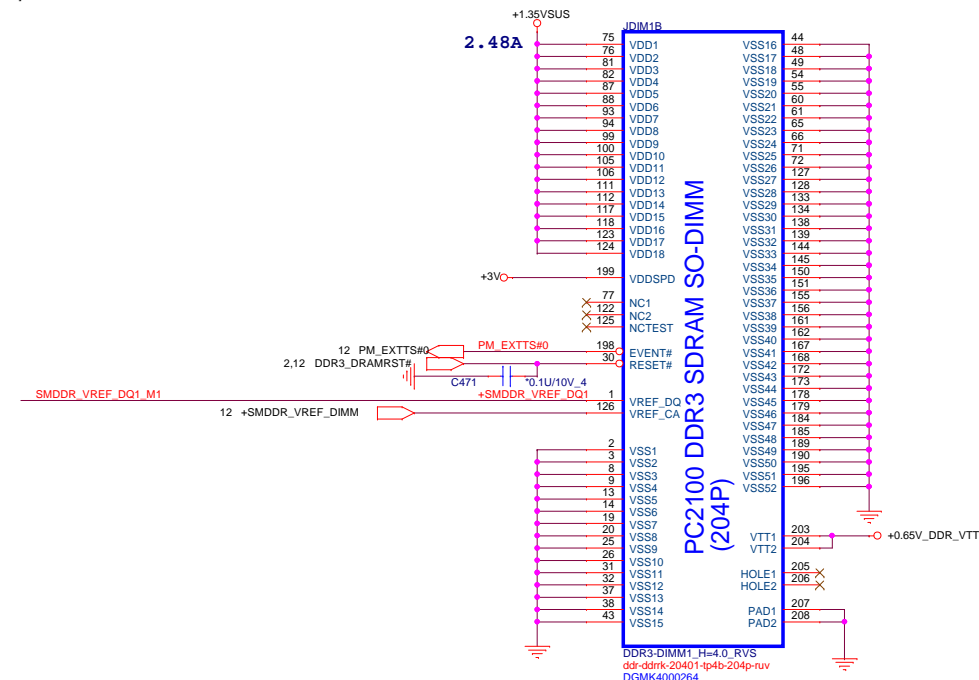


## DIMM &amp; Footprint 同Joshua提供

M\_B\_DQ[63:0] 3



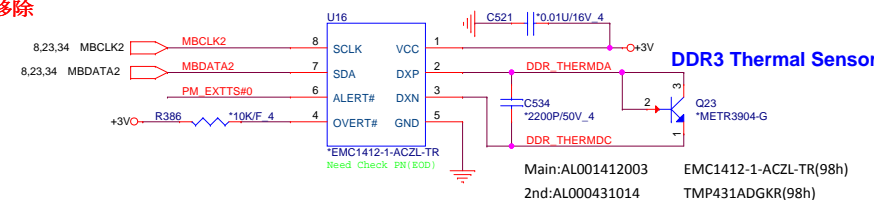
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ddr-ddr3k-20401-tp4b-204p-ruv  
DGMK4000264



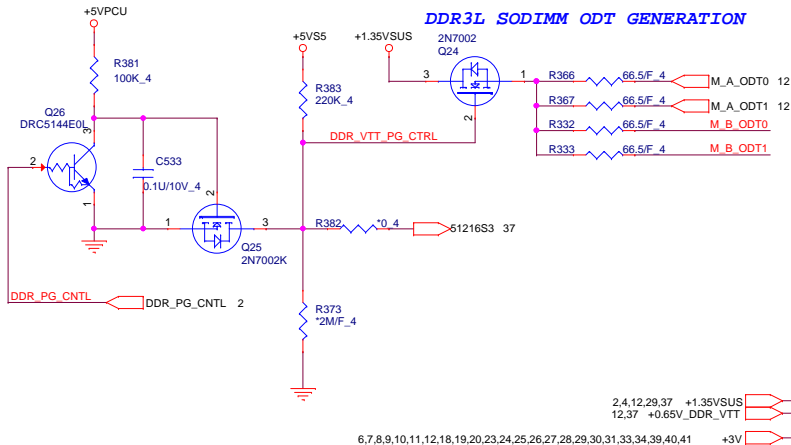
DDR3-DIMM1\_H=4.0\_RVS  
ddr-ddr3k-20401-tp4b-204p-ruv  
DGMK4000264

## Local Thermal Sensor

mv可移除

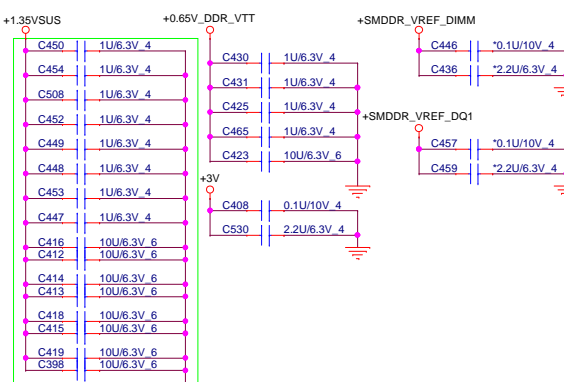



## DDR3L SODIMM ODT GENERATION



## Place these Caps near So-Dimm1.


1uF/10uF 4pcs on each side of connector





**PROJECT :Y05**  
Quanta Computer Inc.


Size Custom	Document Number <b>N15S-GT (PCIE VF) /NVDD</b>	Rev 2A
Date: Wednesday, April 02, 2014		Sheet 14 of 44



**PROJECT :Y05**  
Quanta Computer Inc.

Size Custom	Document Number <b>N15S-GT (MEMORY/GND)</b>	Rev 2A
Date: Wednesday, April 02, 2014		Sheet 15 of 44






**PROJECT :Y05**  
Quanta Computer Inc.

Size Custom	Document Number <b>N15S-GT (DISPLAY)</b>	Rev 2A
Date: Wednesday, April 02, 2014		Sheet 16 of 44

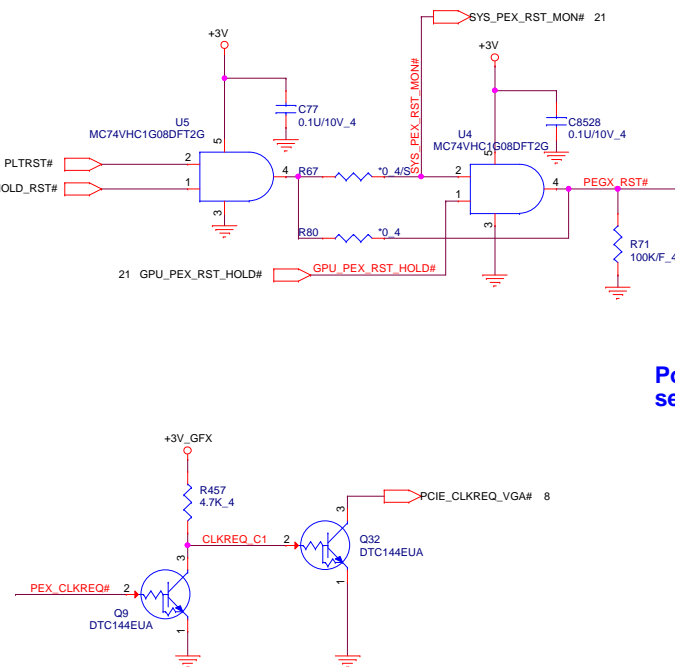
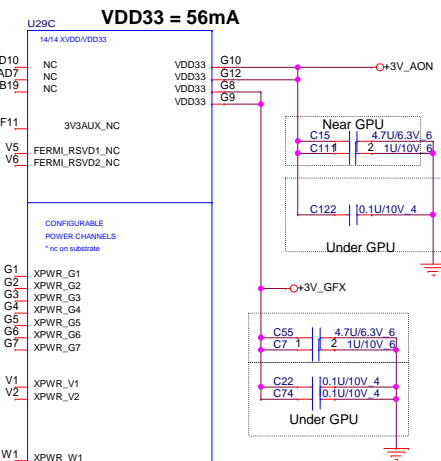
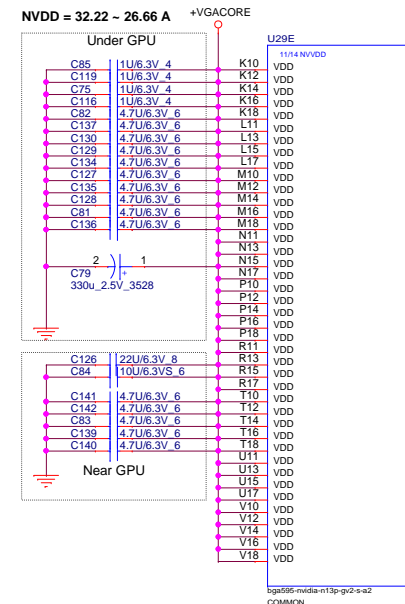
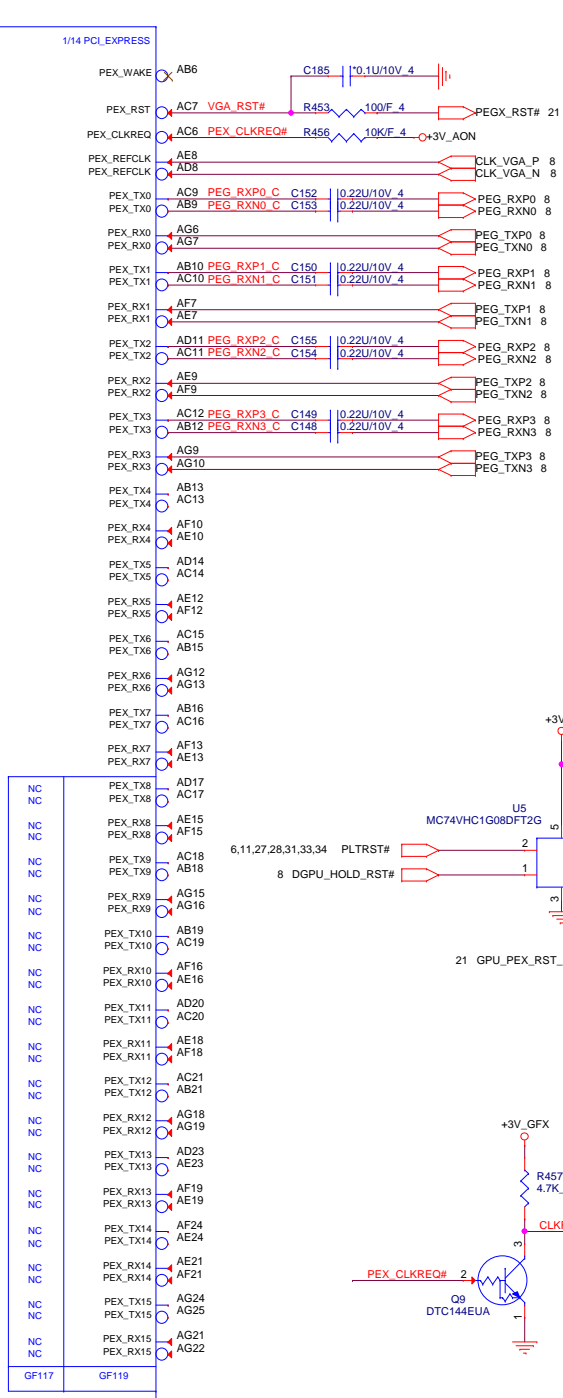
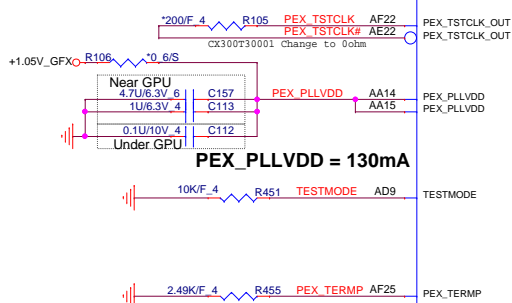
1	2	3	4	5	6	7	8
A							
B							
C							
D							
1	2	3	4	5	6	7	8



**PROJECT :Y05**  
 Quanta Computer Inc.

Size Custom	Document Number <b>N15S-GT (GPIO/STRAPS)</b>	Rev 2A
Date: Wednesday, April 02, 2014		Sheet 17 of 44

1.05V, GFX0				
C191	*22U/6.3V 6	AA10	PEX_10VDD0	
C196	*22U/6.3V 6	AA12	PEX_10VDD0	
C195	*10U/6.3V 6	AA13	PEX_10VDD0	
C187	*10U/6.3V 6	AA18	PEX_10VDD0	
C183	4.7U/6.3V 6	AA19	PEX_10VDD0	
Near GPU		AA20	PEX_10VDD0	
		AA21	PEX_10VDD0	
		AB22	PEX_10VDD0	
		AC23	PEX_10VDD0	
Under GPU		AD24	PEX_10VDD0	
C147	*1U/6.3V 4	AE25	PEX_10VDD0	
C144	*0.1U/10V 4	AF26	PEX_10VDD0	
		AF27	PEX_10VDD0	



## +3.3V\_GFX

NVDD  
+VCC\_DGFX\_COR

FBVDDQ  
+1.5V\_GFX

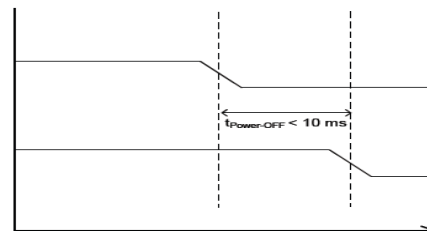
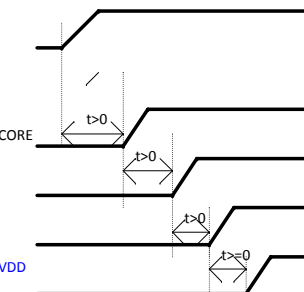
PEX\_VDD  
+1.05V\_GFX

IFP(CDEF)\_IOVDD  
+1.05V\_GFX

## First Rail

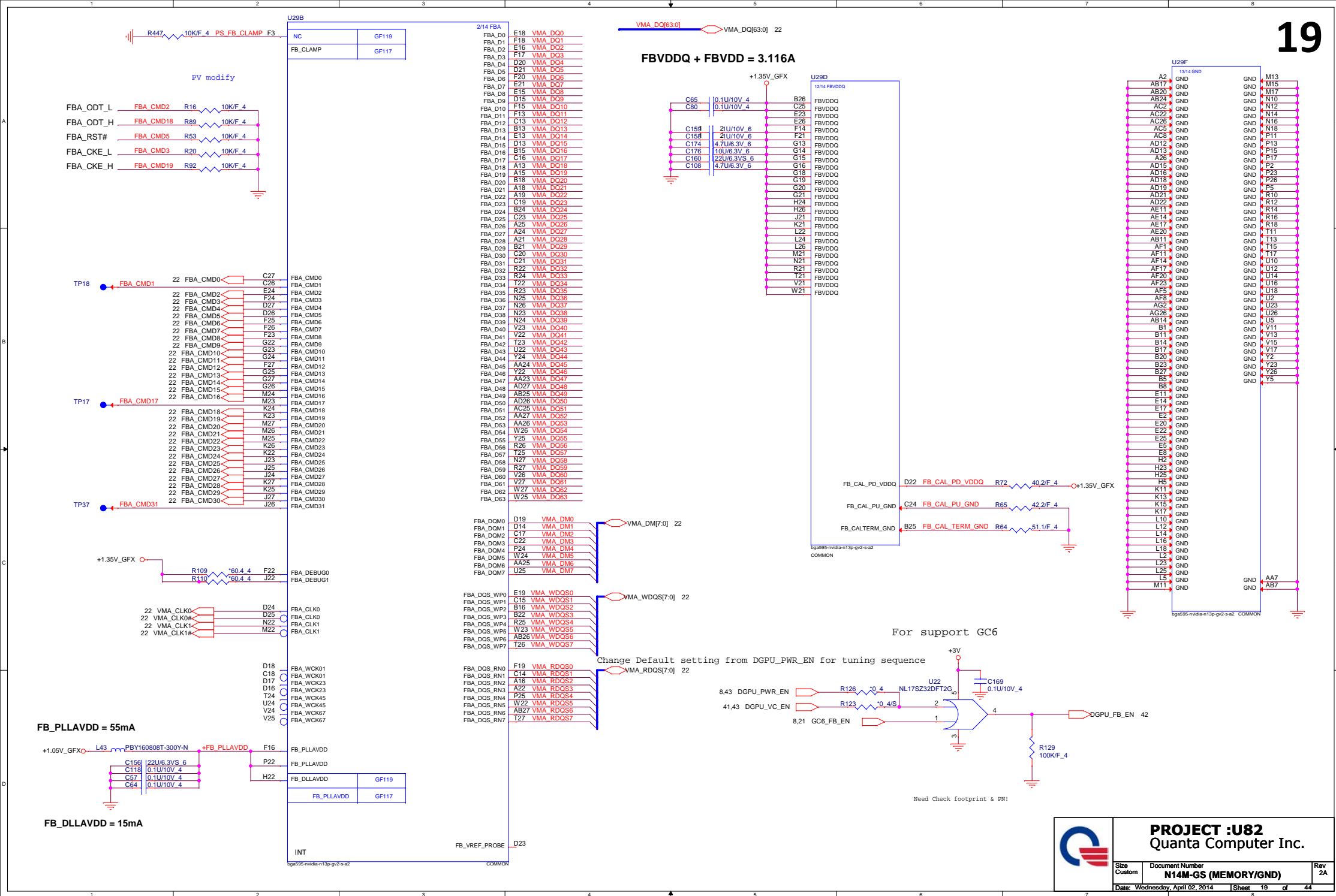
First Rail  
to Power  
Down

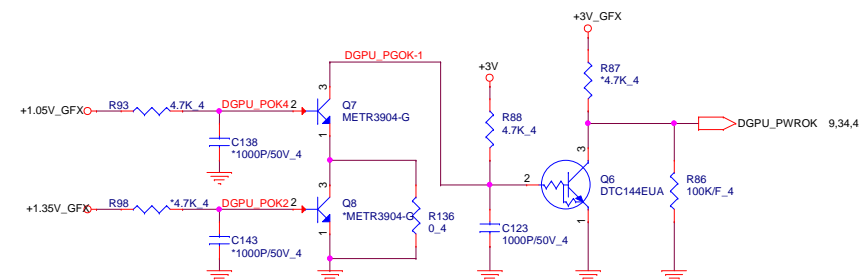
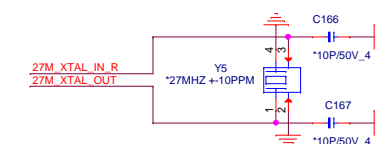
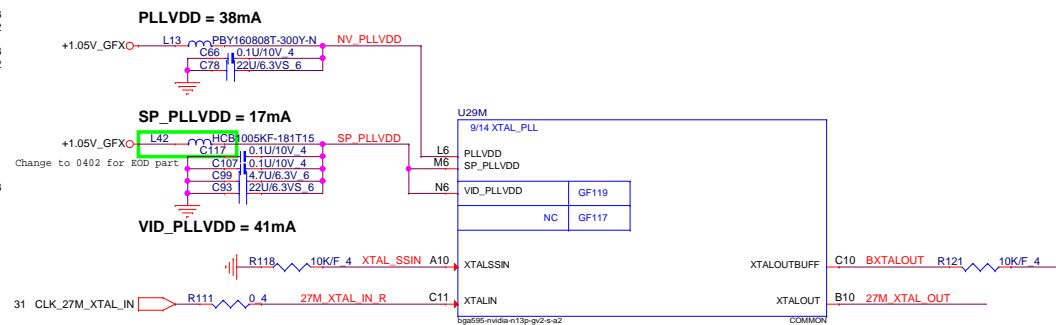
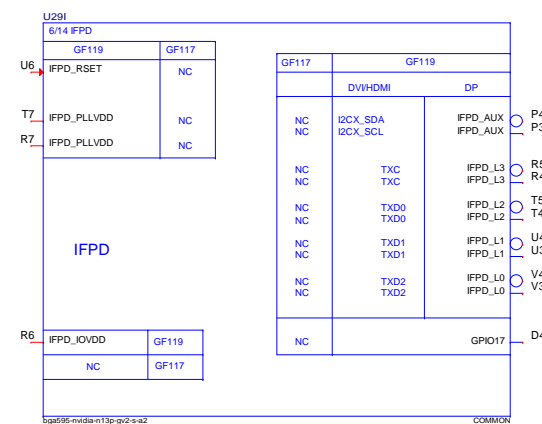
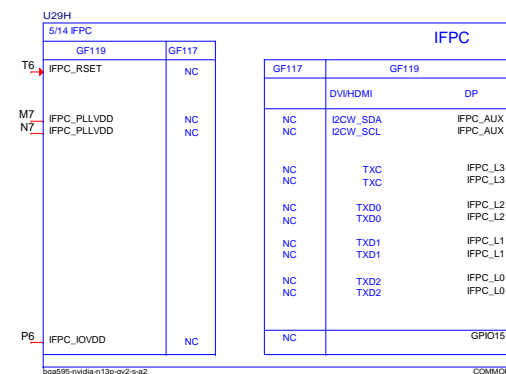
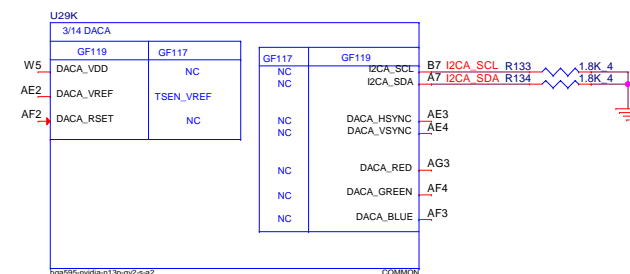
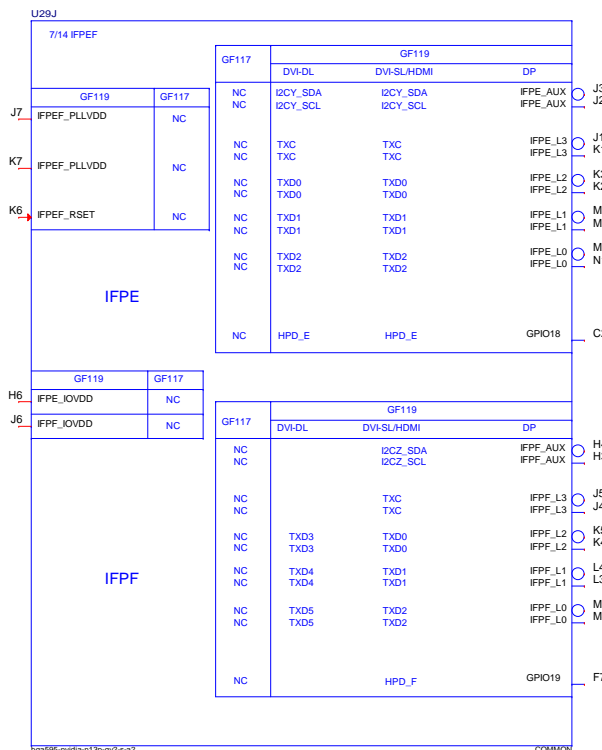
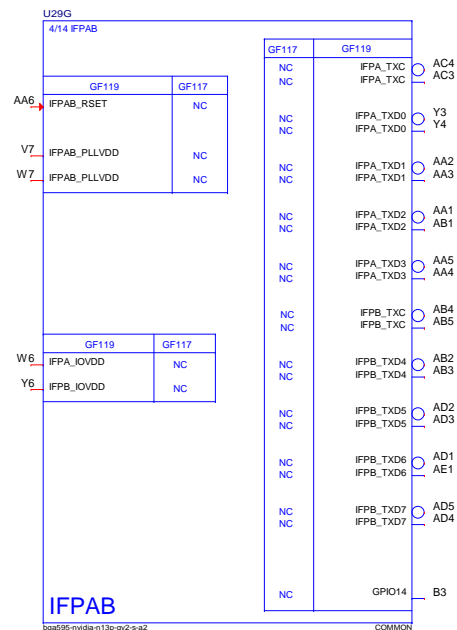
Last Rail t  
Power  
Down



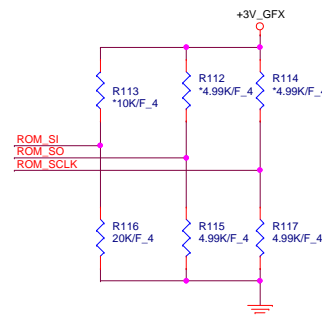
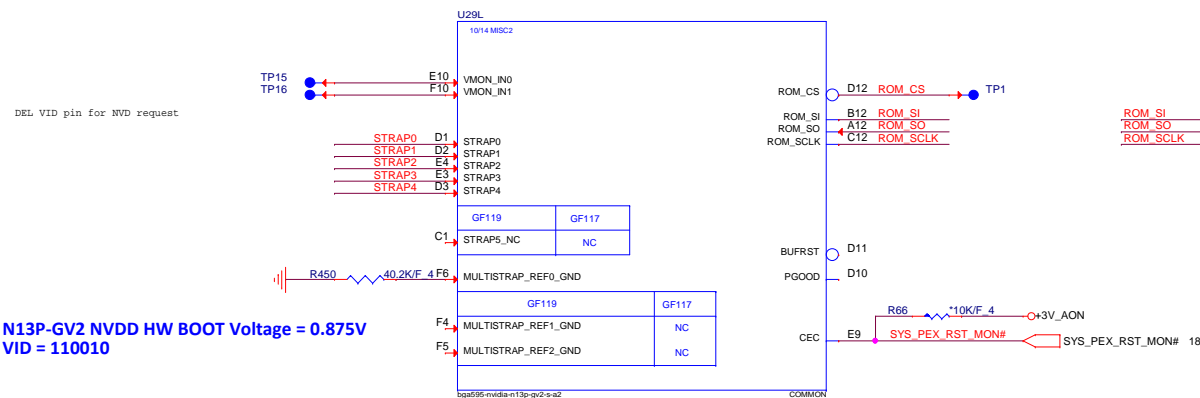
**PROJECT :U82**  
Quanta Computer Inc.

Size Custom	Document Number <b>N14M-GS (PCIE VF) /NVDD</b>	Rev 2A
Date: Wednesday, April 02, 2014		Sheet 18 of 44

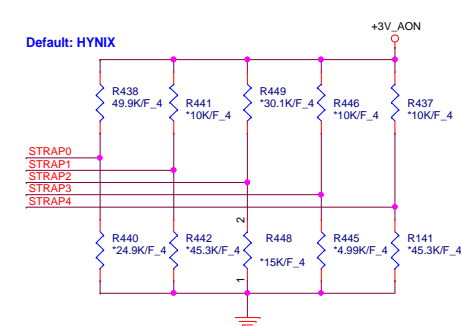




N13P-GV2 NVDD HW BOOT Voltage = 0.875V  
VID = 110010



Default: HYNIX

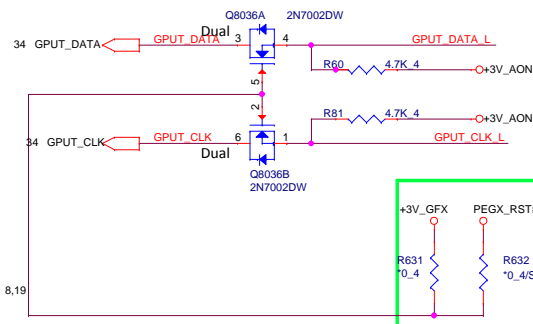
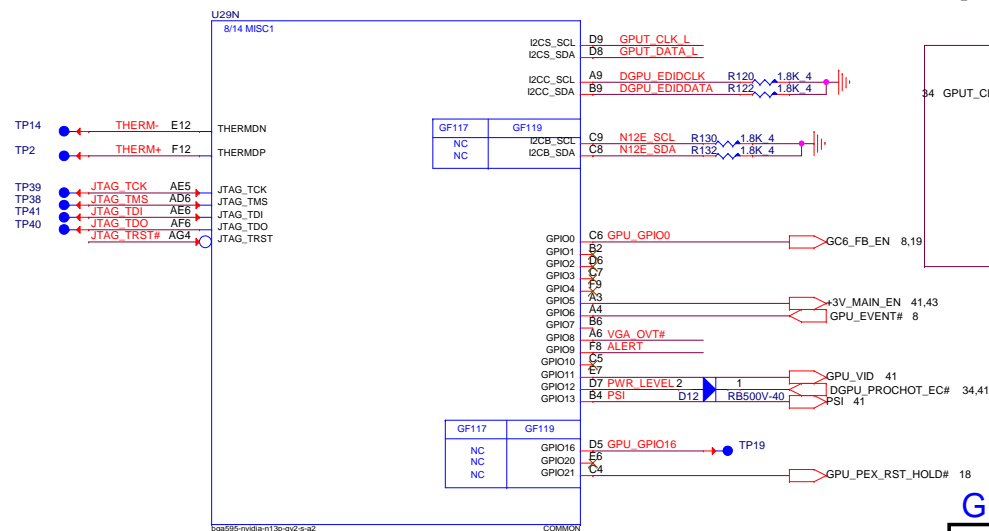


4.99k CS24992PB26  
10k CS31002PB26  
15k CS31502PB24  
20k CS32002PB29  
24.9k CS32492PB16  
30.1k CS33012PB18  
34.8k CS33482PB22  
45.3k CS34532PB18

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Hynix should be 0x3, R440 20K 1%  
Micro Should be 0x4, R440 24.9K 1%  
Samsung Should be 0x5, R440 30.1K 1%

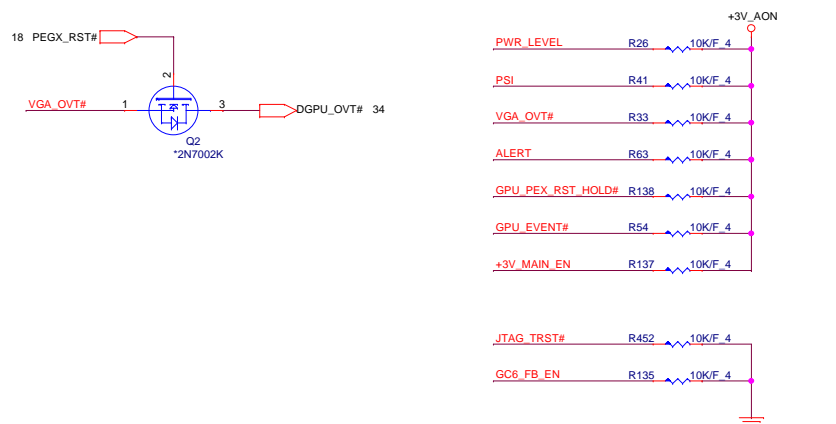


VRAM Configuration Table ROM\_SI

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	QBC	TOP B/S
0000	DDR3 256Mx16, 64bit, 4Gb,900MHz	...	MT41J256M16HA-093G:B	S-M	AKD5PZSTL01	AKD5PZSTL00
0100	DDR3 256Mx16, 64bit, 4Gb,900MHz	Micron	H5TC4G63AFR-11C	AKD5PGWT500	AKD5PGWTW08	AKD5PGWTW07
0011	DDR3 256Mx16, 64bit, 4Gb,900MHz	HYNIX	4W4G1646D-BC1A			
0101		SAMSUNG				

## GPIO ASSIGNMENTS

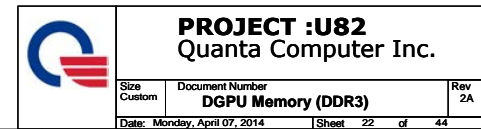
GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



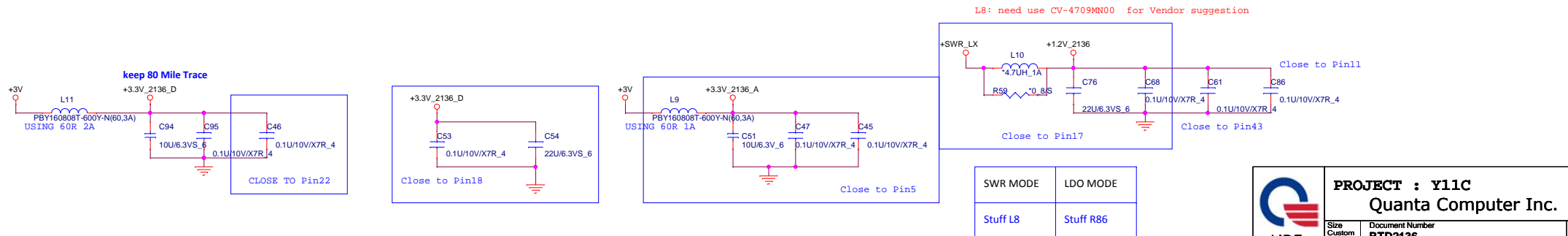
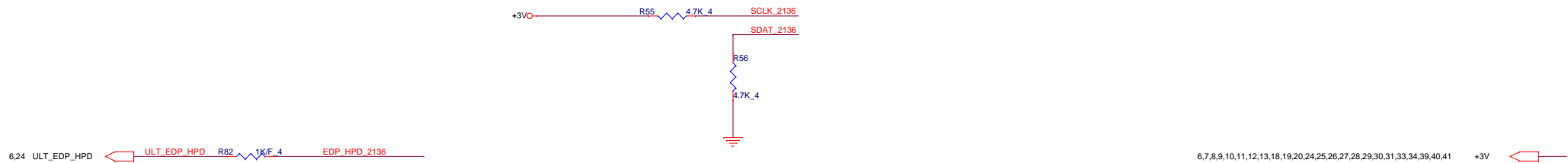
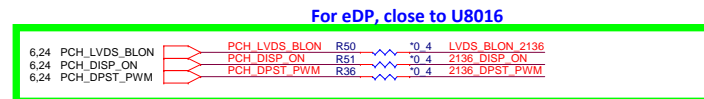
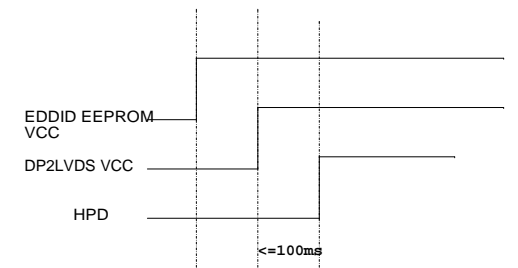
**PROJECT :U82**  
Quanta Computer Inc.

Size Custom Document Number **N14M-GS (GPIO/STRAPS)** Rev 2A

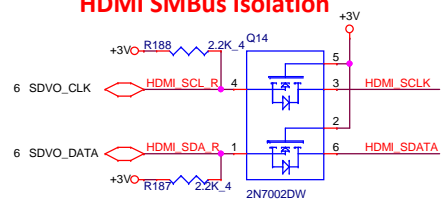
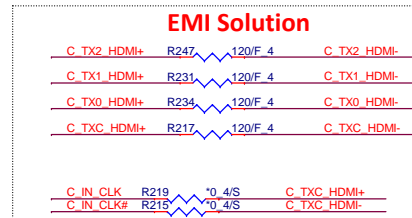
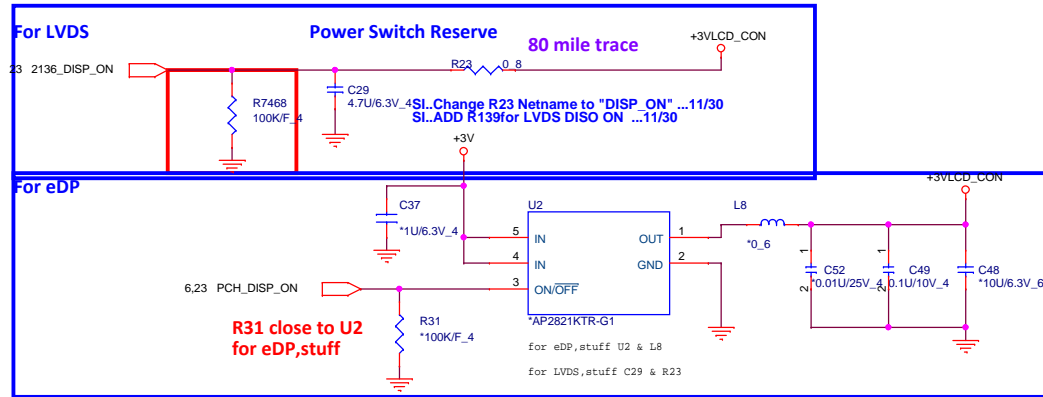
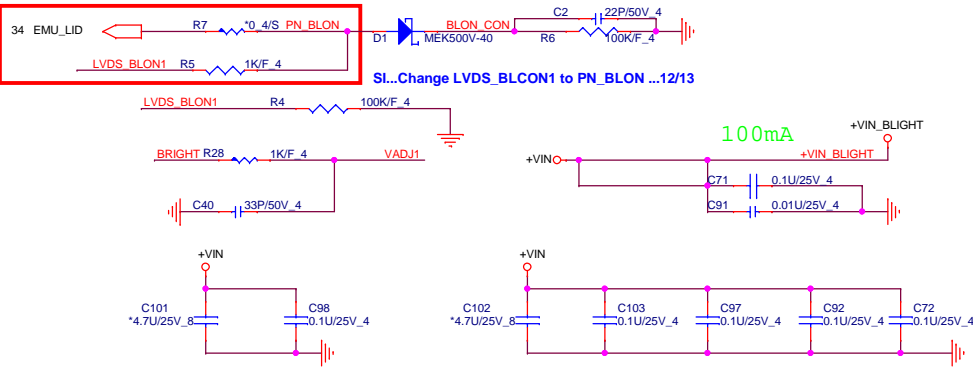
Date: Tuesday, April 08, 2014 Sheet 21 of 44



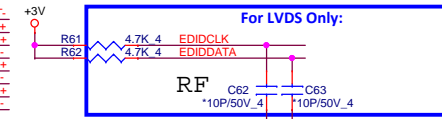
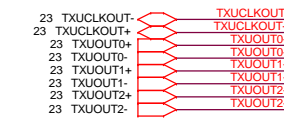
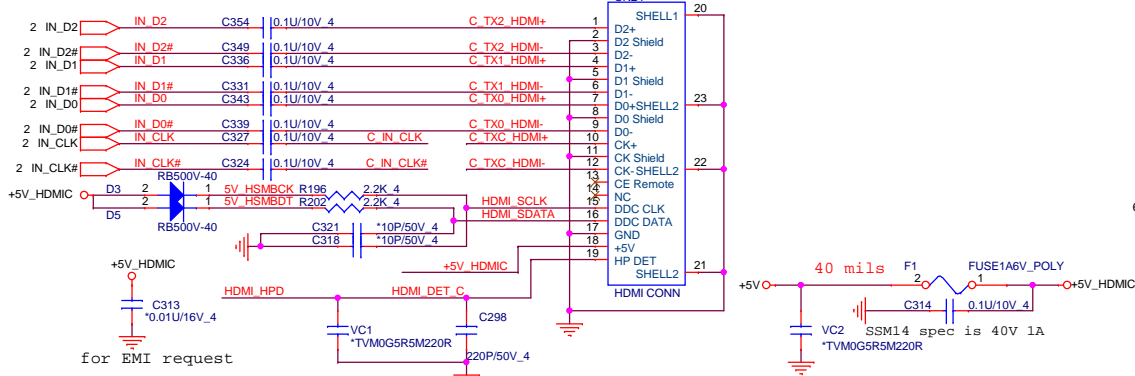
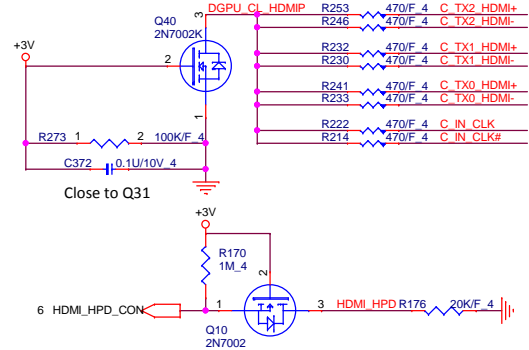




## LID Switch

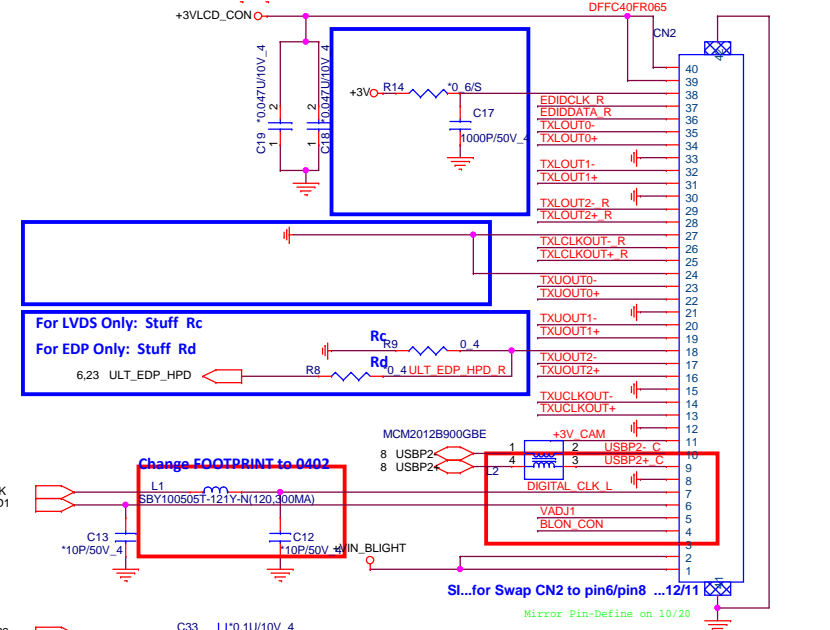


For EDP Only: stuff Cap  
For LVDS only stuff Resistor

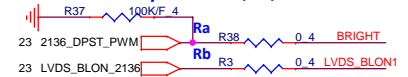


**LVDS Conn.**

24



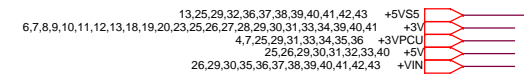
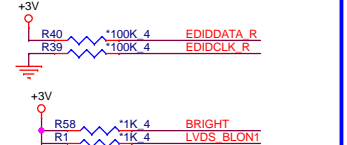
For LVDS Only: stuff Ra,Rb,Rc



For EDP Only: stuff Rd,Re,Rf



**For EDP Only: stuff**

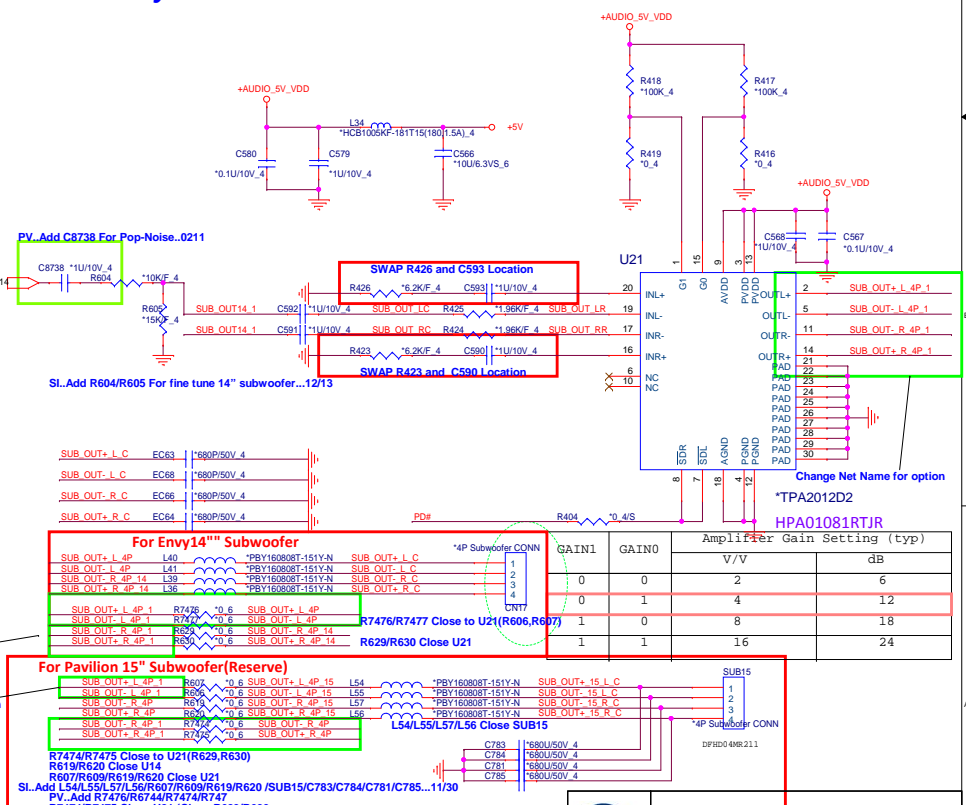



**PROJECT : Y11C**  
**Quanta Computer Inc.**

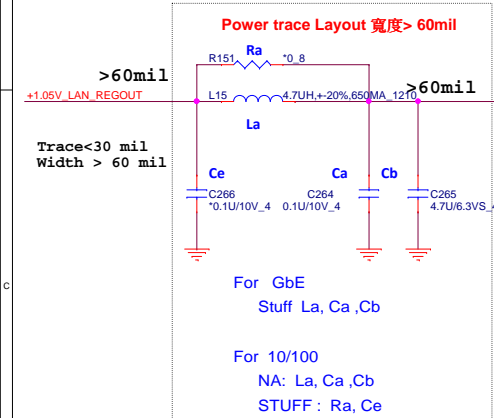
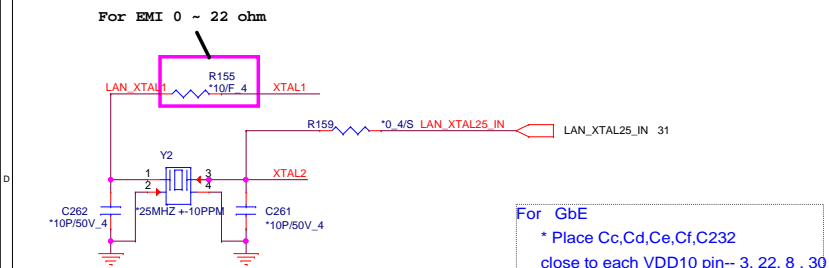
Size Custom	Document Number <b>LCD CONN/LID/CAM/D-MIC</b>	Rev 1A
Date: Monday, April 07, 2014	Sheet 24	of 44



**For Pavilion 15" Subwoofer(Reserve)  
For Envy14"" Subwoofer**



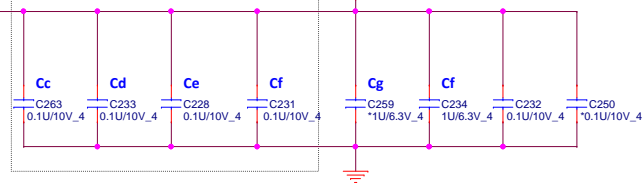
 NB5	<b>PROJECT : Y11C</b> <b>Quanta Computer Inc.</b>		
	Size C	Document Number <b>Card Reader</b>	Rev 1A
Date: Wednesday, April 02, 2014		Sheet 26 of 44	



For GbE

- \* Place Cc,Cd,Ce,Cf,C232 close to each VDD10 pin-- 3, 22, 8 , 30

For 10/100 NA Ce,Cf  
 \* Place Ce , Cf ,C250  
 close to each VDD10 pin-- 8, 30 only,



For GbE

- \* Place Cf close to each VDD10 pin-- 22 (reserve)

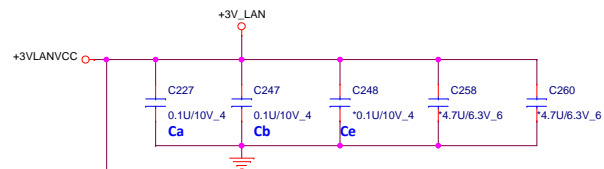
\* Place  $C_g$  close to each VDD10 pin-- 30 (reserve)

For 10/100

- \* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA

- \* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32

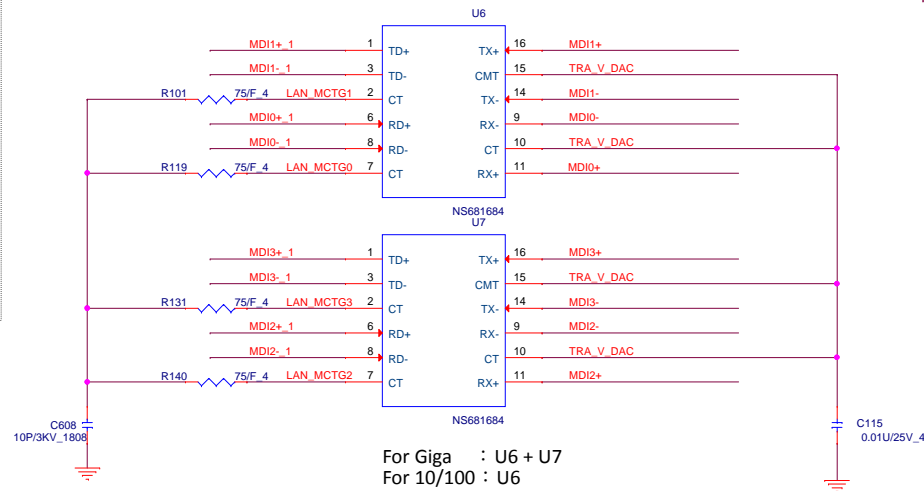
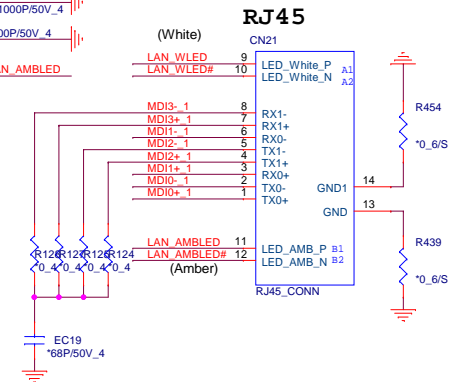
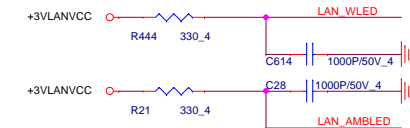
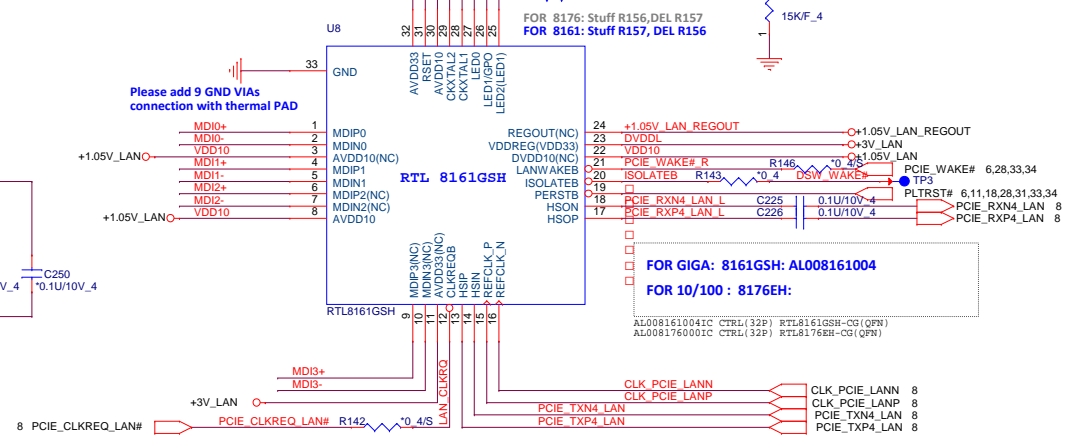


\* Place Cc and Cd close to each VDD33 pin-- 23

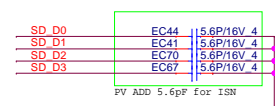
For GIGA  
Stuff Cc, Cd

For 10/100  
NA: Cc, Cd

Remove For Not Using SWR mode



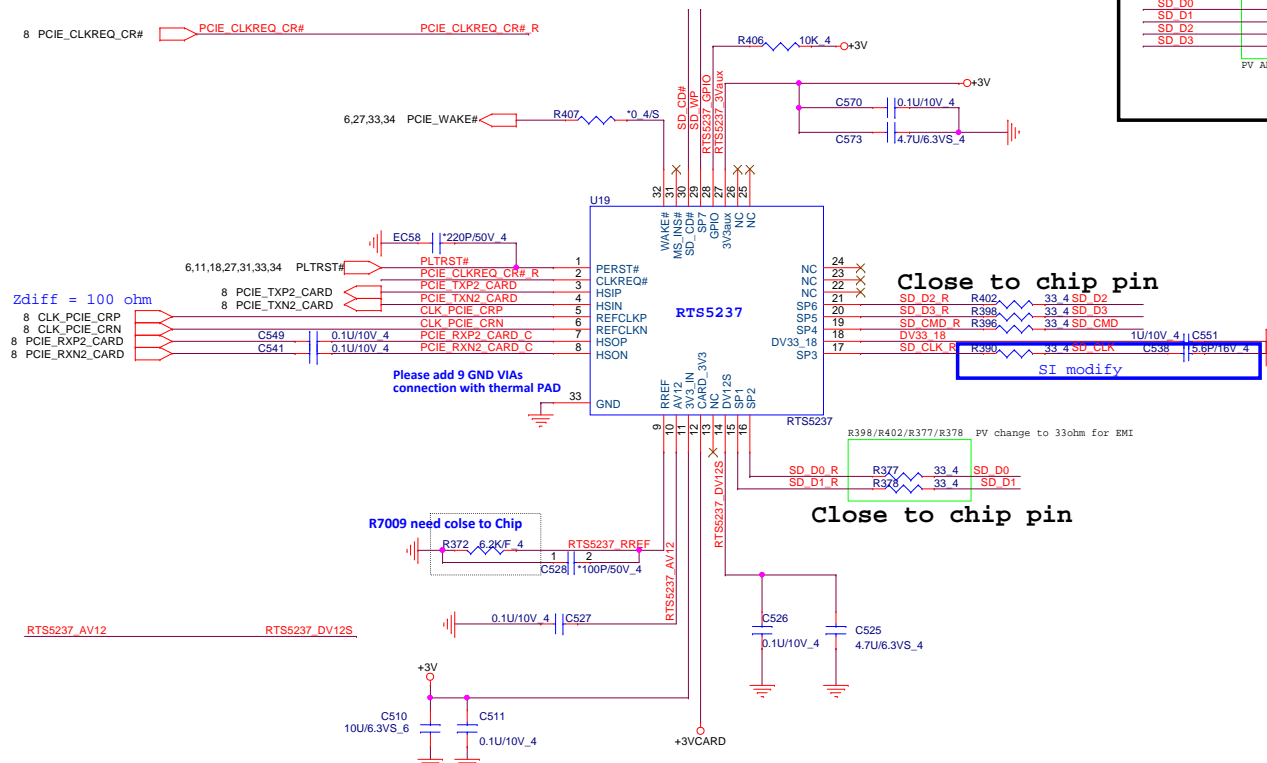
Reserve for EMI



SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

## Share Pin

SD / MMC

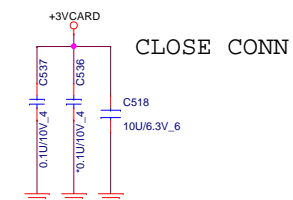


NC 24 ✗  
NC 23 ✗  
NC 22 ✗

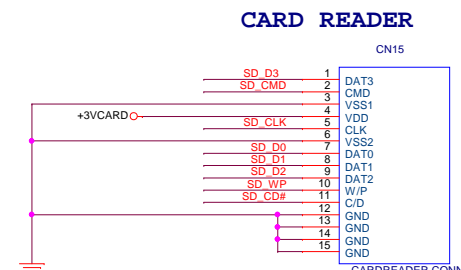
Close to chip pin

SI modify

Close to chip pin



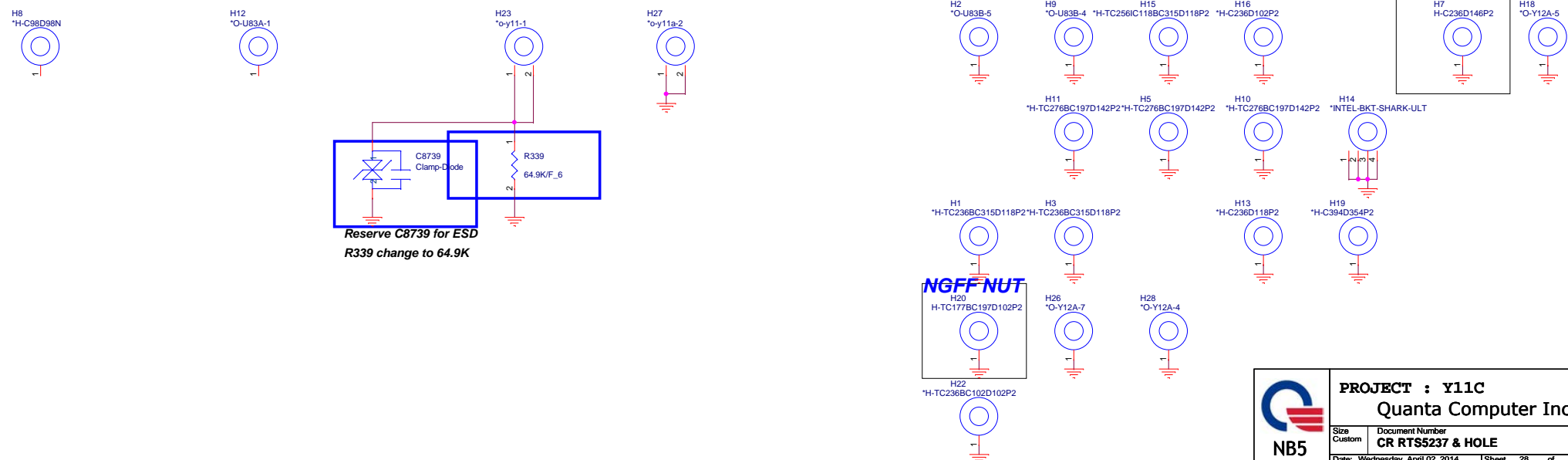
CLOSE CONN



CARD READER

R6x Type

## Thermal Nut



**Reserve C8739 for ESD**  
**R339 change to 64.9K**

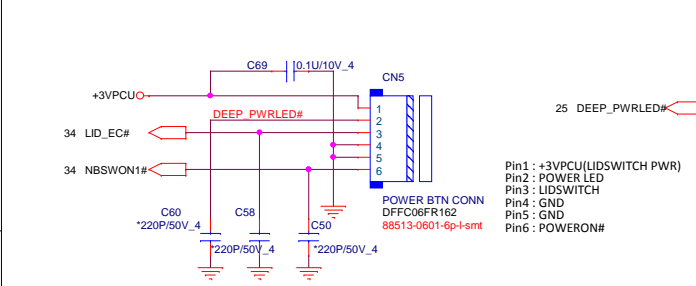
**NGFF NUT**



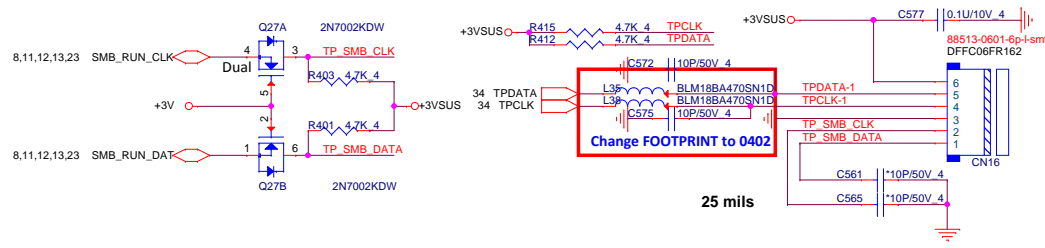
PROJECT : Y11C  
Quanta Computer Inc.

Size Custom	Document Number <b>CR RTS5237 &amp; HOLE</b>
Date: Wednesday, April 02, 2014	Sheet 28 of 44

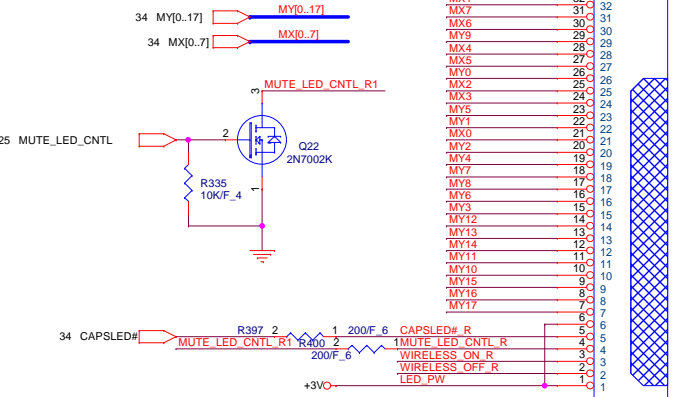
# Power Button Connector



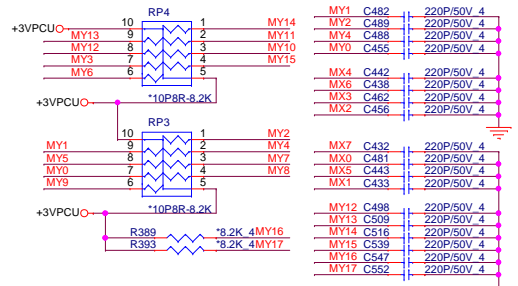
# Touch Pad Connector



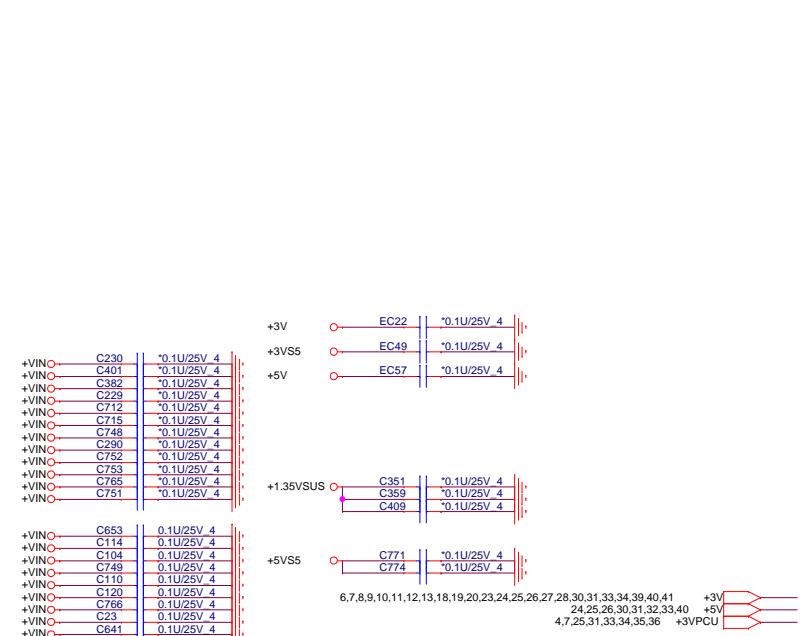
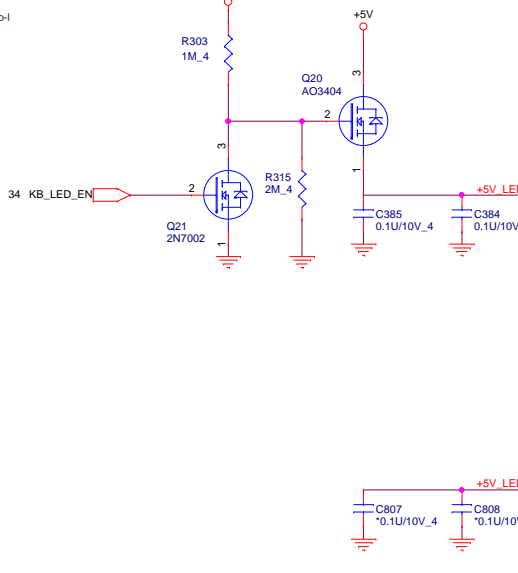
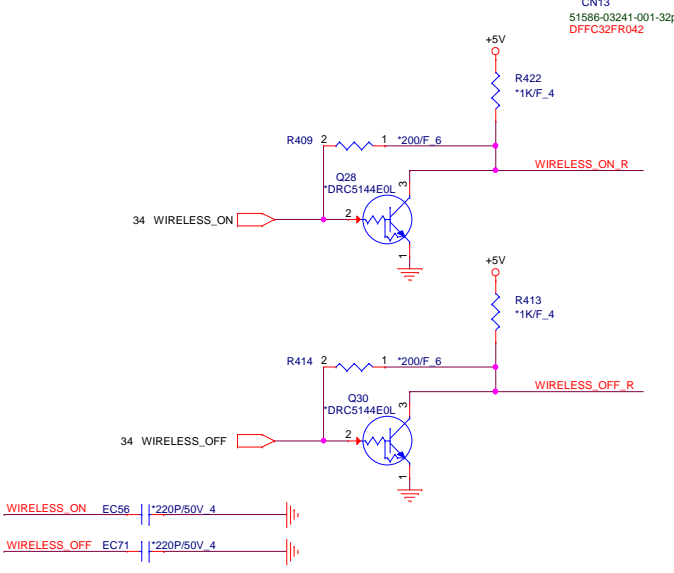
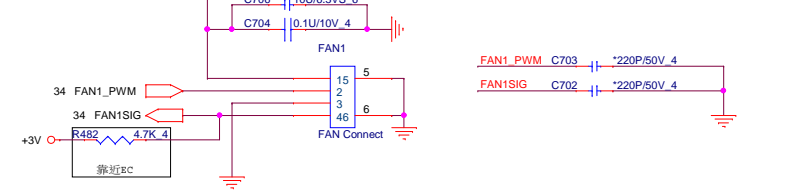
# KEYBOARD Con.



# KEYBOARD PULL-UP



# FAN



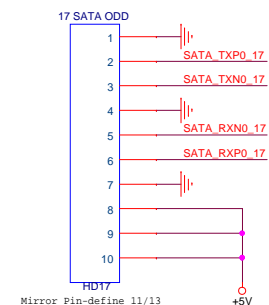
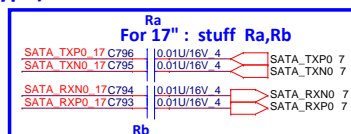
**PROJECT : Y11C**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	PB/TP/KB/FAN/EMI Cap	1A
Date: Wednesday, April 02, 2014	Sheet 29 of 44	

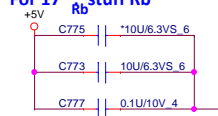


## HDD

## SATA HDD Connector(Cable type) 15.6"

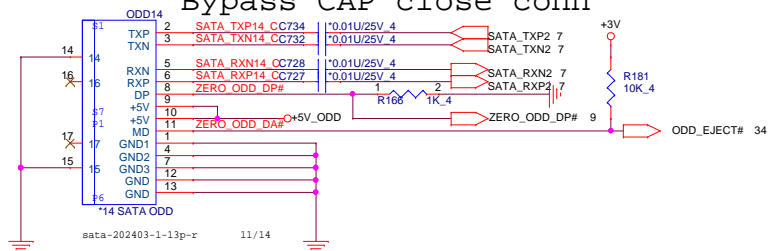


For 17" : stuff Rb

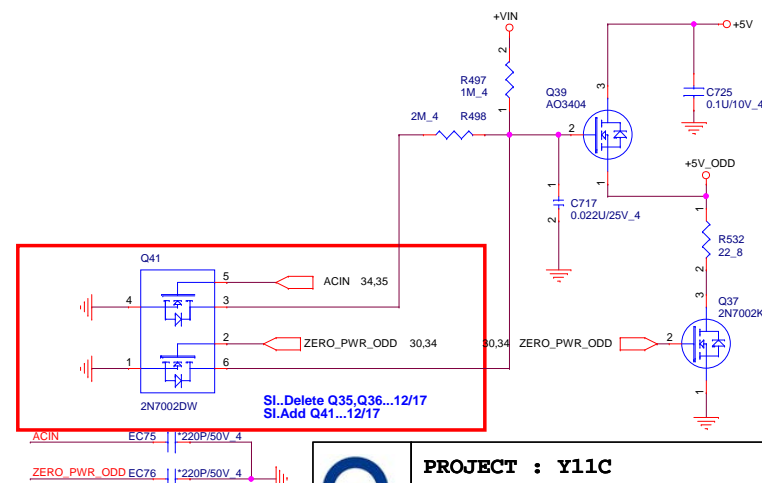
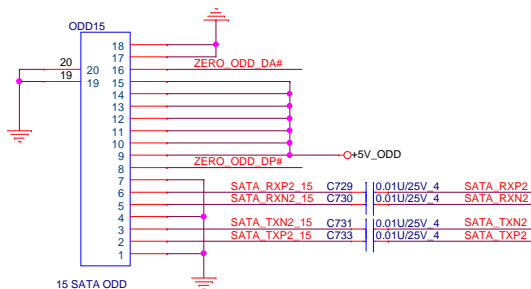
SATA ODD  
CONNECTOR

## 14" SATA ODD

Bypass CAP close conn



## 15" SATA ODD



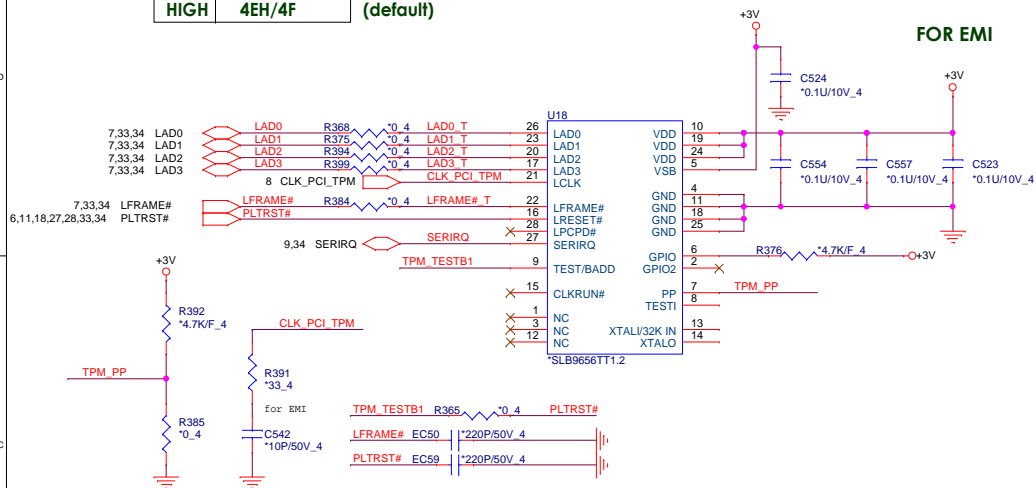
High : ODD power down  
Low : ODD power on

		<b>PROJECT : Y11C</b>	
		<b>Quanta Computer Inc.</b>	
Size Custom	Document Number <b>HDMI</b>	Rev 1A	
Date: Wednesday, April 02, 2014		Sheet	30 of 44

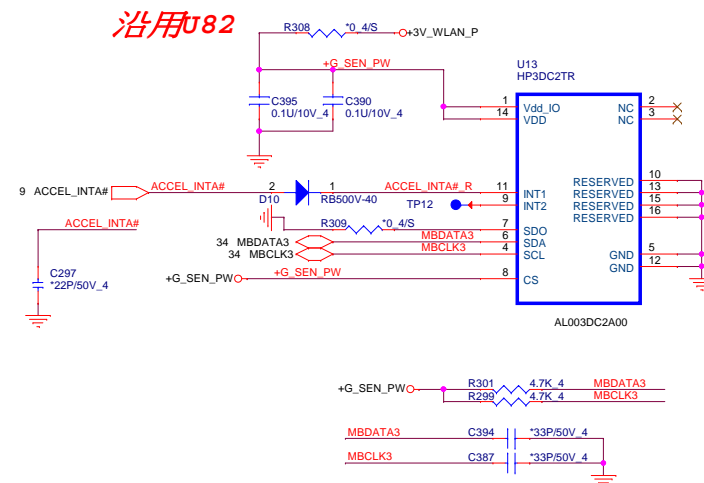
## TPM (1.2)

**Address**

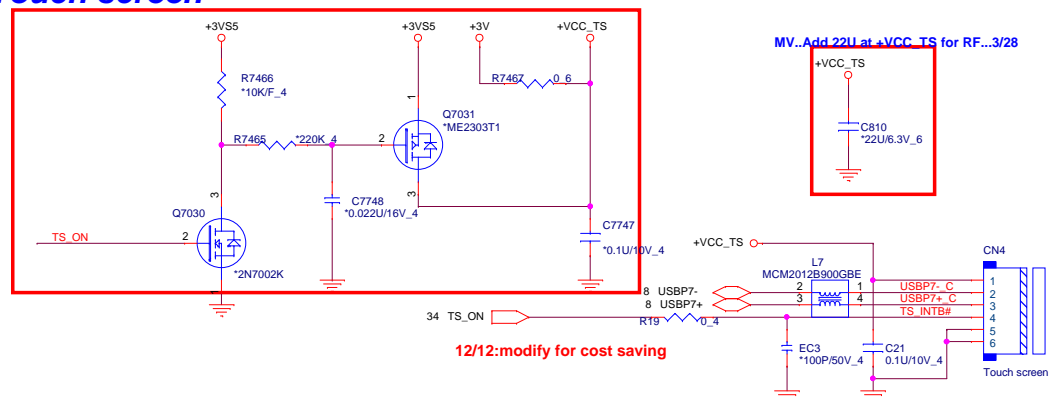
	<b>BADD</b>
<b>HIGH</b>	<b>4EH/4F</b> (default)



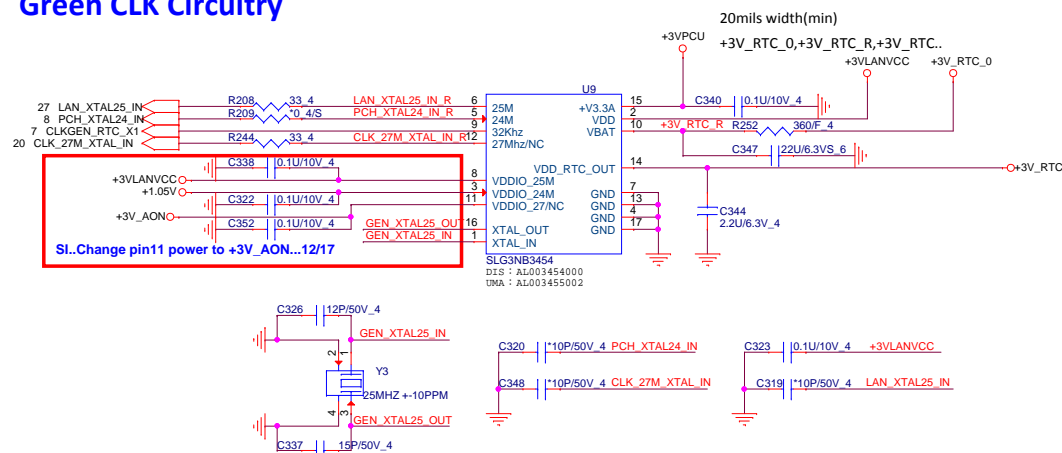
## Accelerometer Sensor



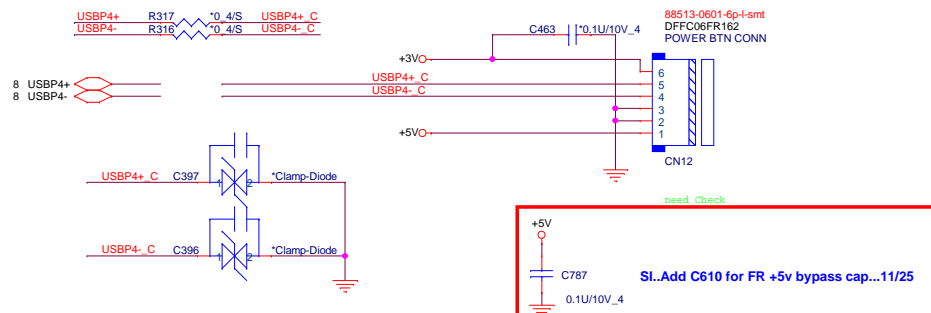
## Touch screen




## Green CLK Circuitry

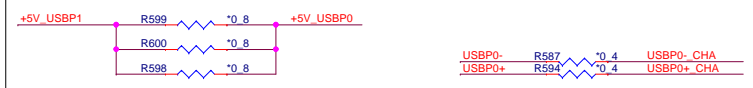


## Fingerprint Conn



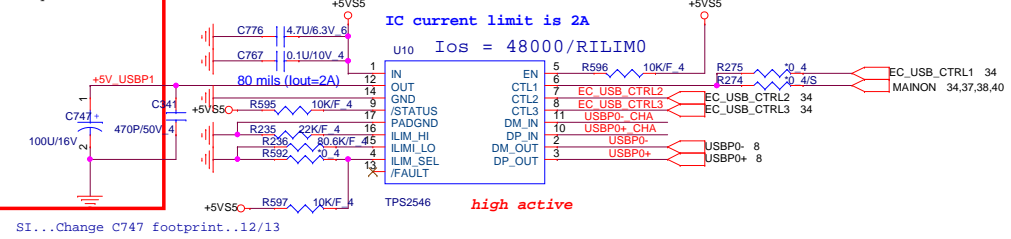
 <b>NB5</b>	<b>PROJECT : Y11C</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>TPM/G-Sensor/G-CLK/TS/FP</b>	Rev 1A
Date: Wednesday, April 02, 2014		Sheet 31 of	44

if Envy SKU,non-staff



For Pavilion / Envy SKU stuff

for Envy SKU stuff



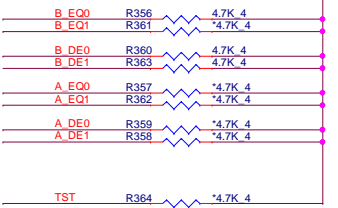
SI...Change C747 footprint..12/13

Right-Side USB3.0 Re-Driver

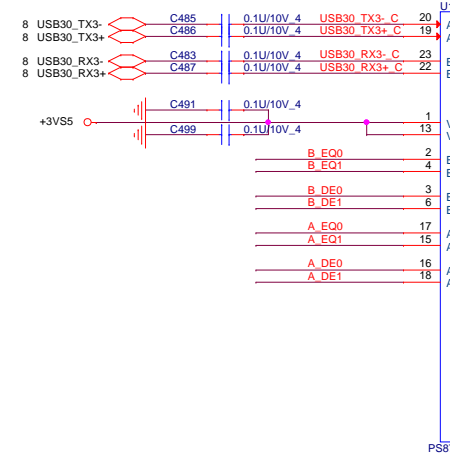
AEQ 9.5db / ADE 3.5db  
BEQ 13db / BDE 5db / REXT 5.36K

A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	7.5dB	1	1	5dB

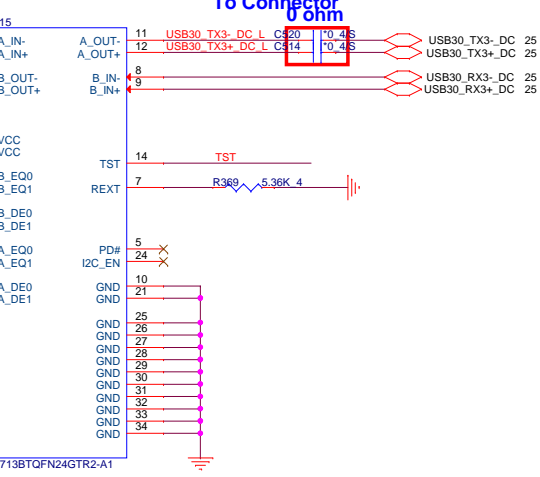
TST : Low = Normal LFPS swing / High =Turn down LFPS swing



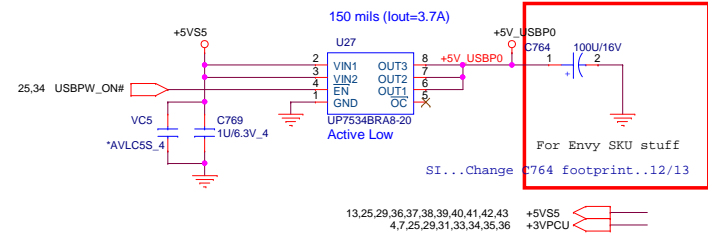
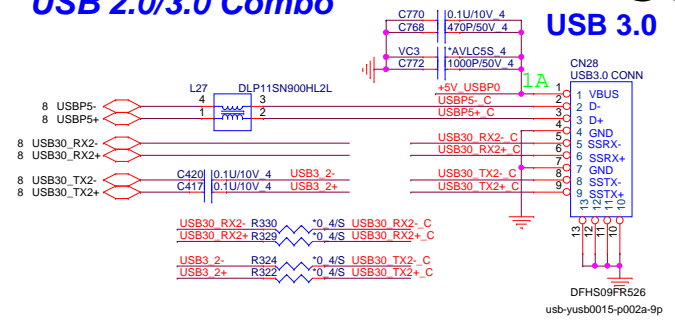
From HOST



USB3.0 Re-driver

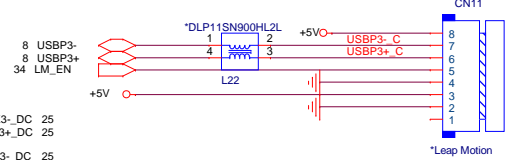



USB 2.0/3.0 Combo



For Envy SKU stuff  
SI...Change C764 footprint..12/13

DFFC08FR016

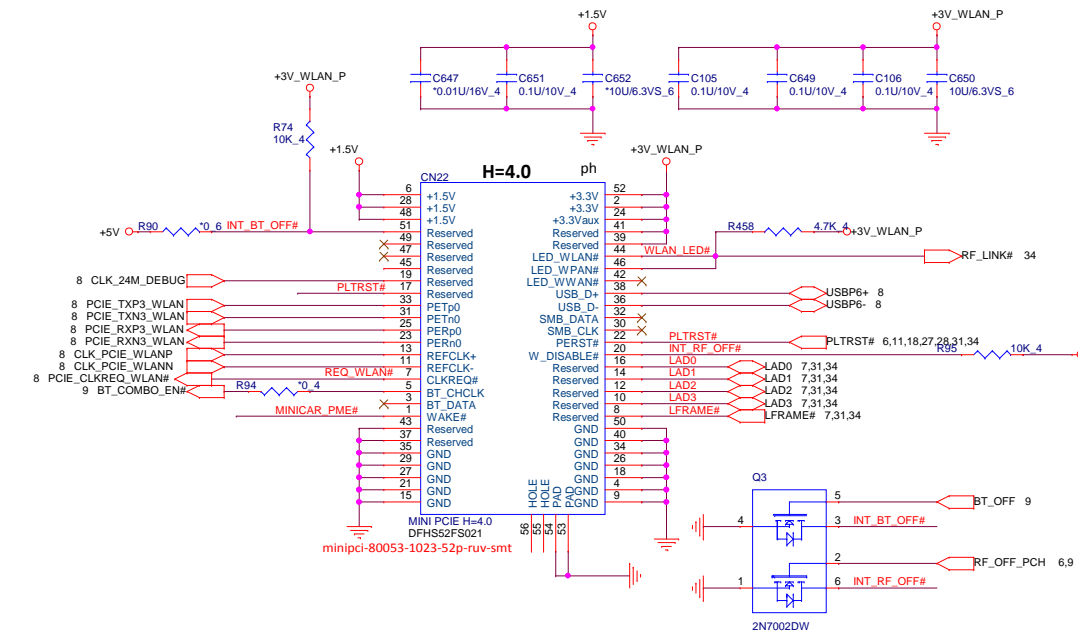




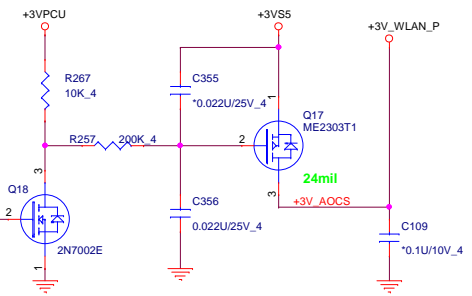
**PROJECT : Y11C**

**Quanta Computer Inc.**

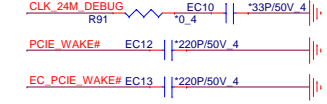
Size Custom	Document Number	Rev 1A
<b>USB 3.0</b>		
Date: Wednesday, April 02, 2014	Sheet 32 of 44	



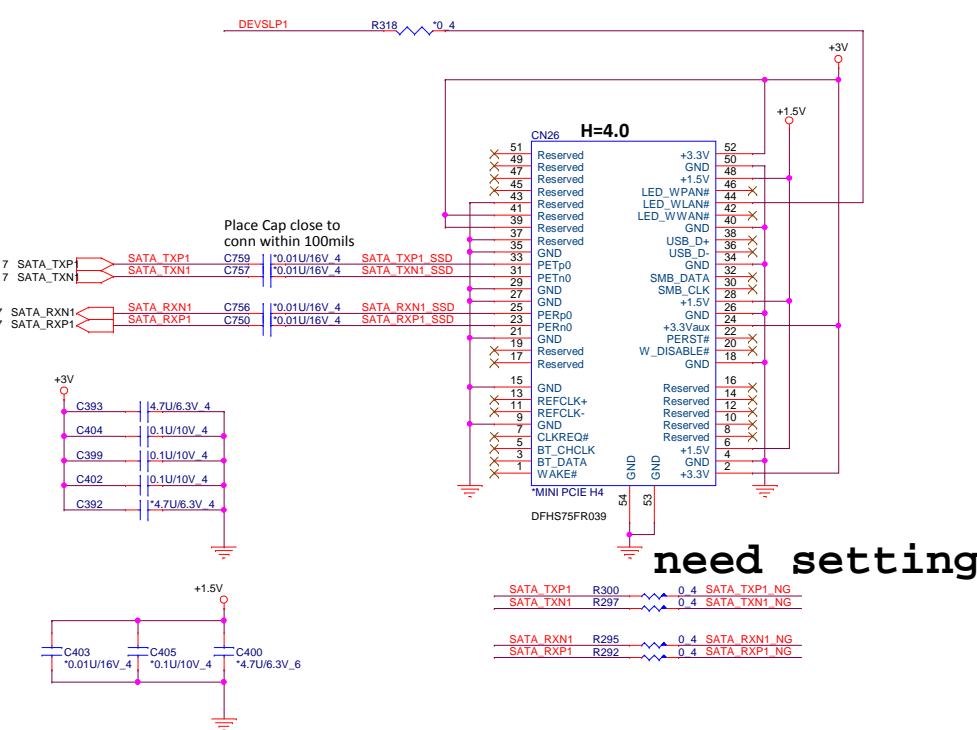
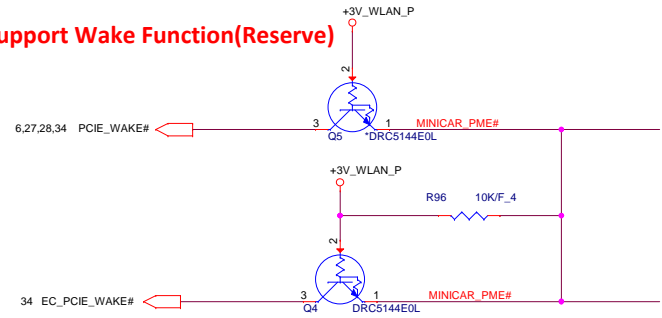
### Mini Card WLAN/BT(Optional)



### For EMI Suggestion

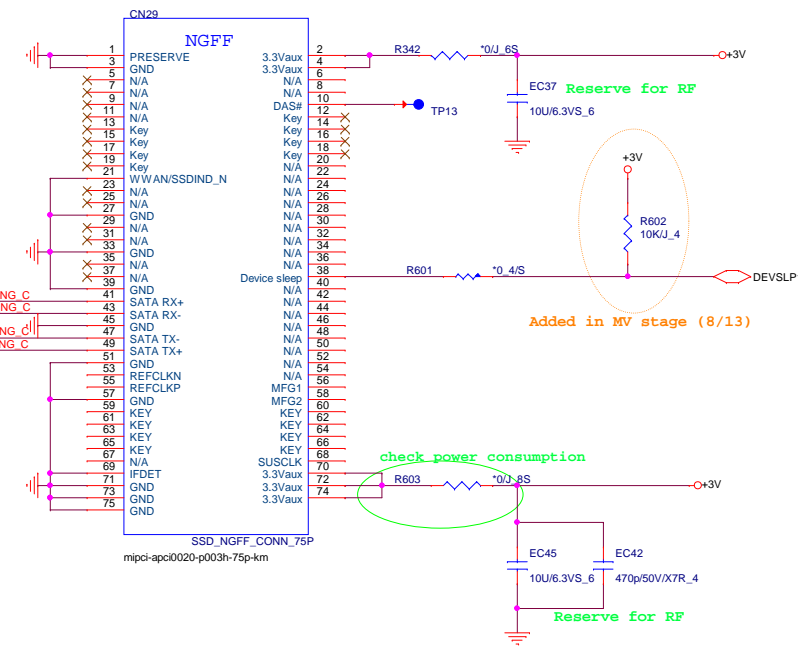


### Support Wake Function(Reserve)



### NGFF-SSD

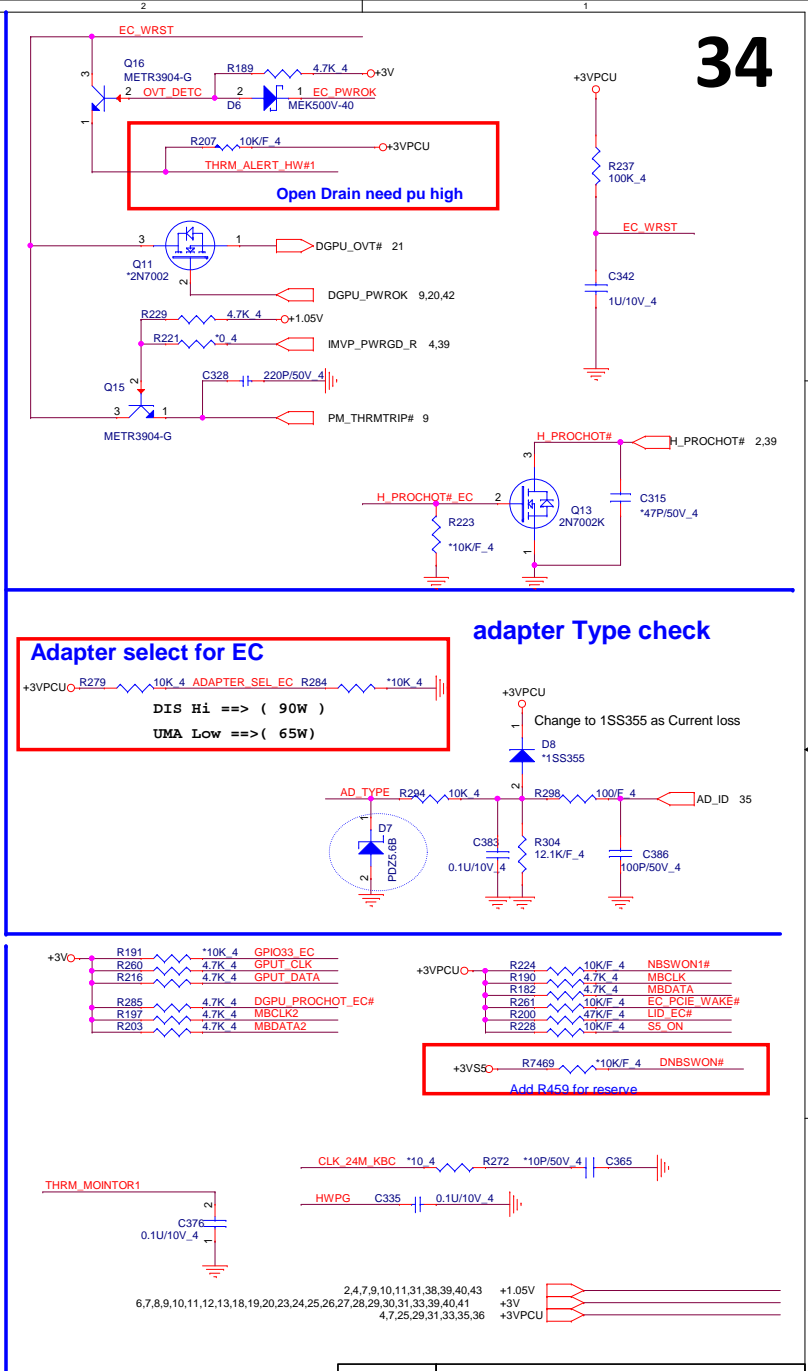
SATA\_RXP1\_NG C778 0.01u25V\_4 SATA\_RXP1\_NG C  
SATA\_RXN1\_NG C779 0.01u25V\_4 SATA\_RXN1\_NG C  
SATA\_TXN1\_NG C780 0.01u25V\_4 SATA\_TXN1\_NG C  
SATA\_TXP1\_NG C782 0.01u25V\_4 SATA\_TXP1\_NG C



need setting

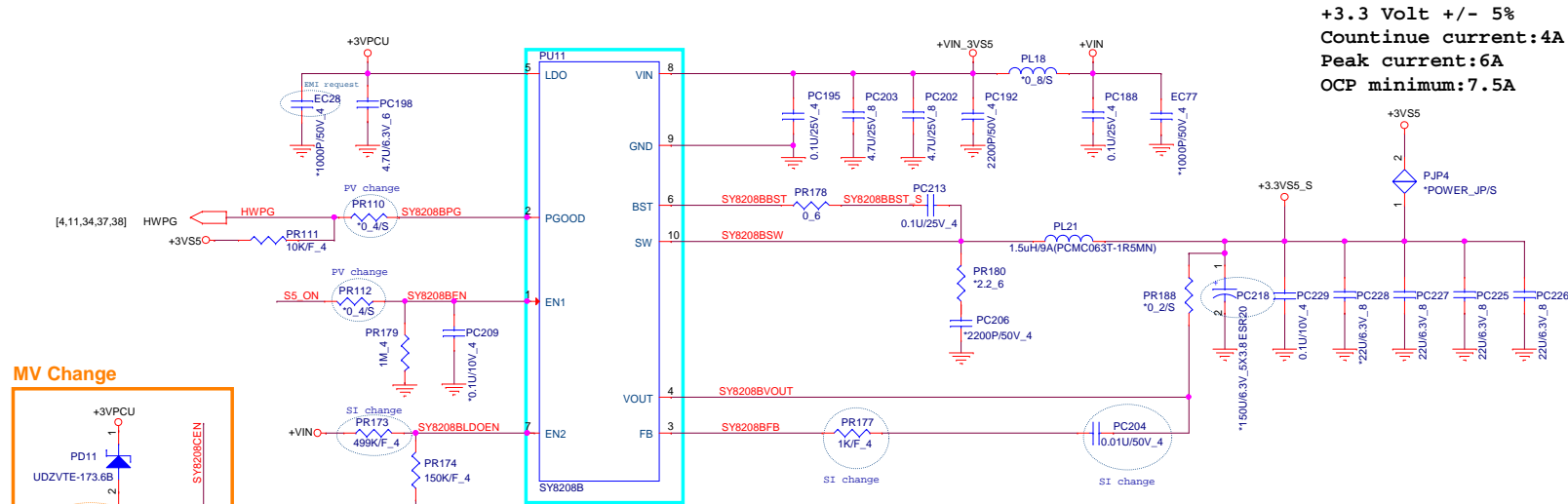
need setting

NB5	PROJECT : Y11C		
	Quanta Computer Inc.		
	Size Custom	Document Number	Rev 1A
	Date: Wednesday, April 02, 2014	WLAN/NGFF/MSATA	33 of 44

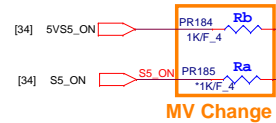
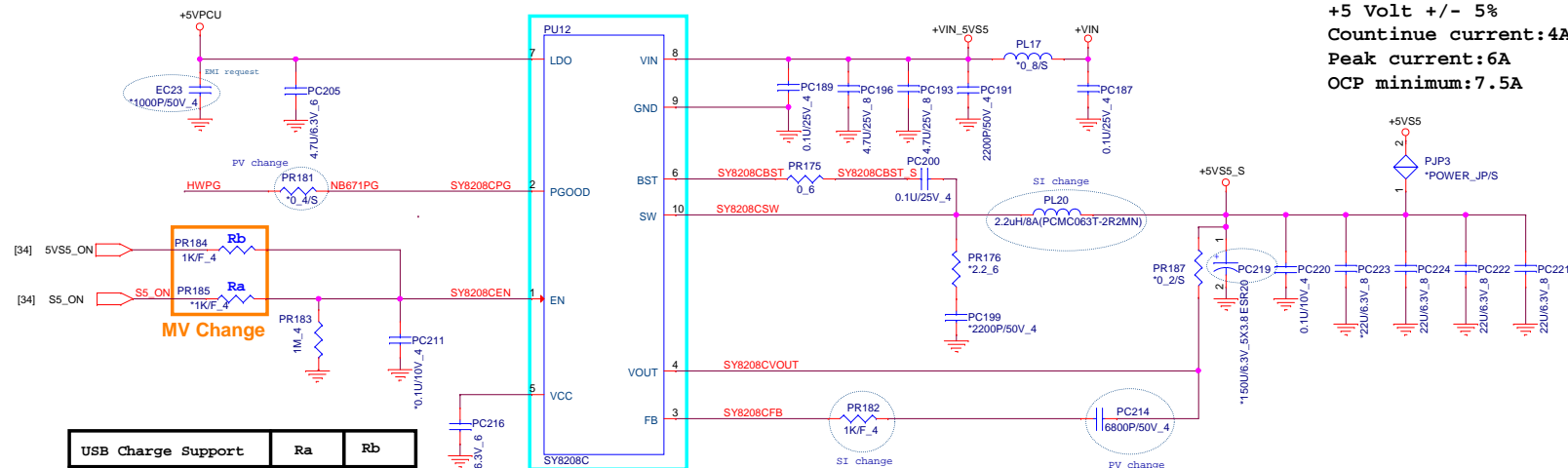
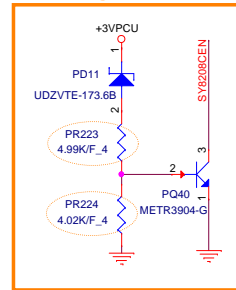





## DC/DC +3VS5/+5VS5



## MV Change

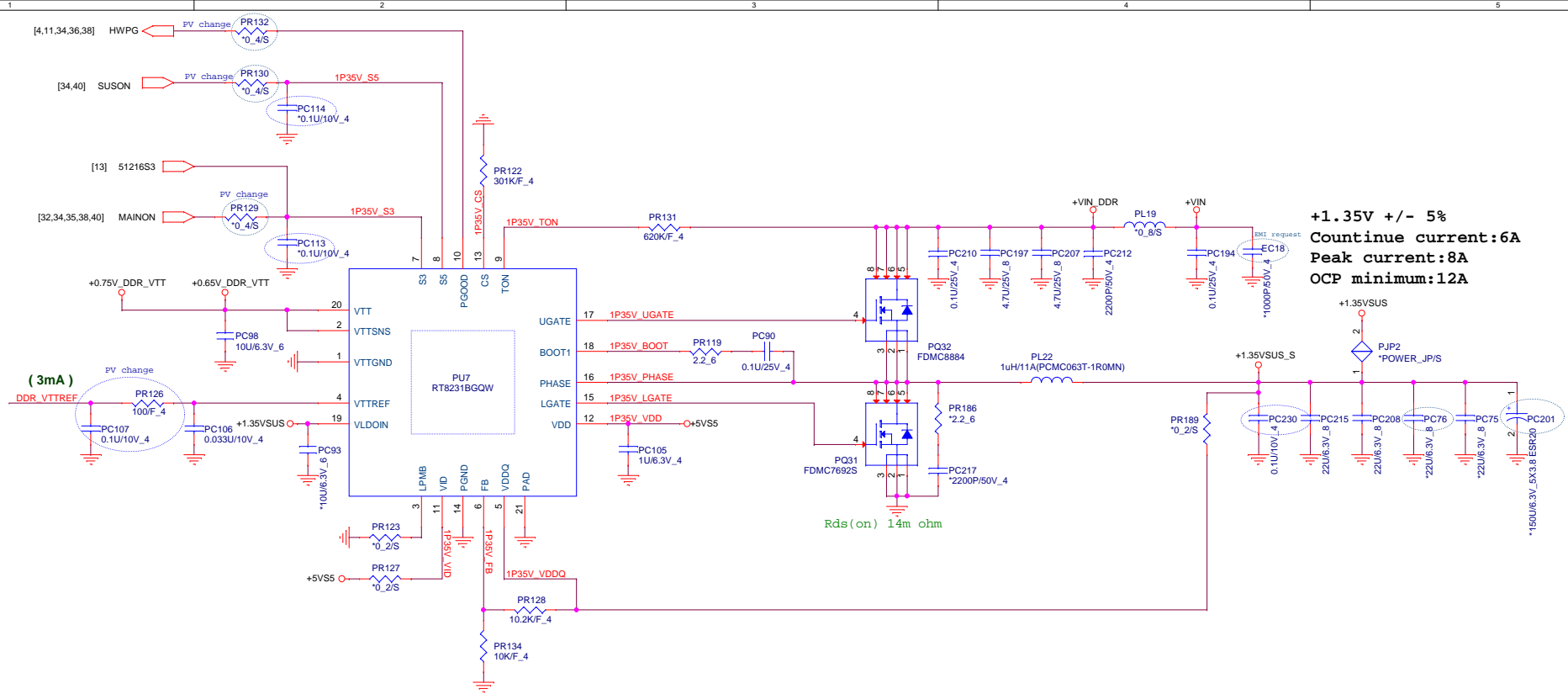


USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

 NB5	PROJECT : R63 Quanta Computer Inc.		
	Size Custom	Document Number <b>3/5VPCU(RT8243A)</b>	Rev 1A
	Date: Wednesday, April 02, 2014	Sheet 36 of 44	

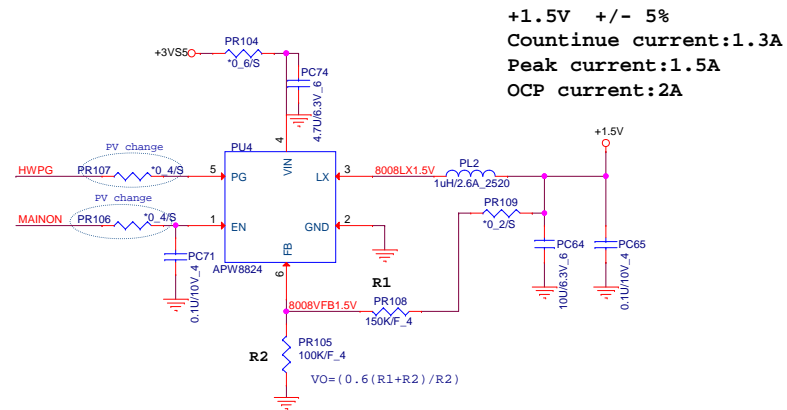
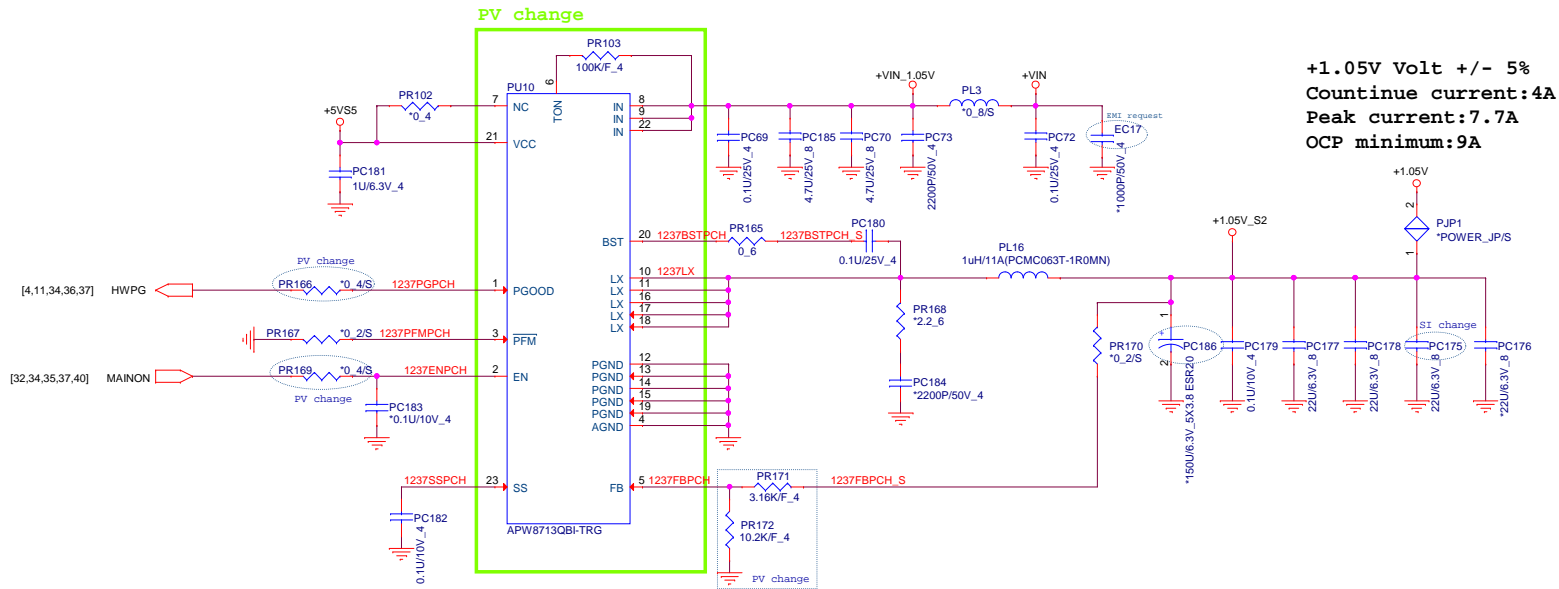


+1.35V +/- 5%  
Continue current: 6A  
Peak current: 8A  
OCP minimum: 12A


 +1.35V SUS [2,4,12,13,29]

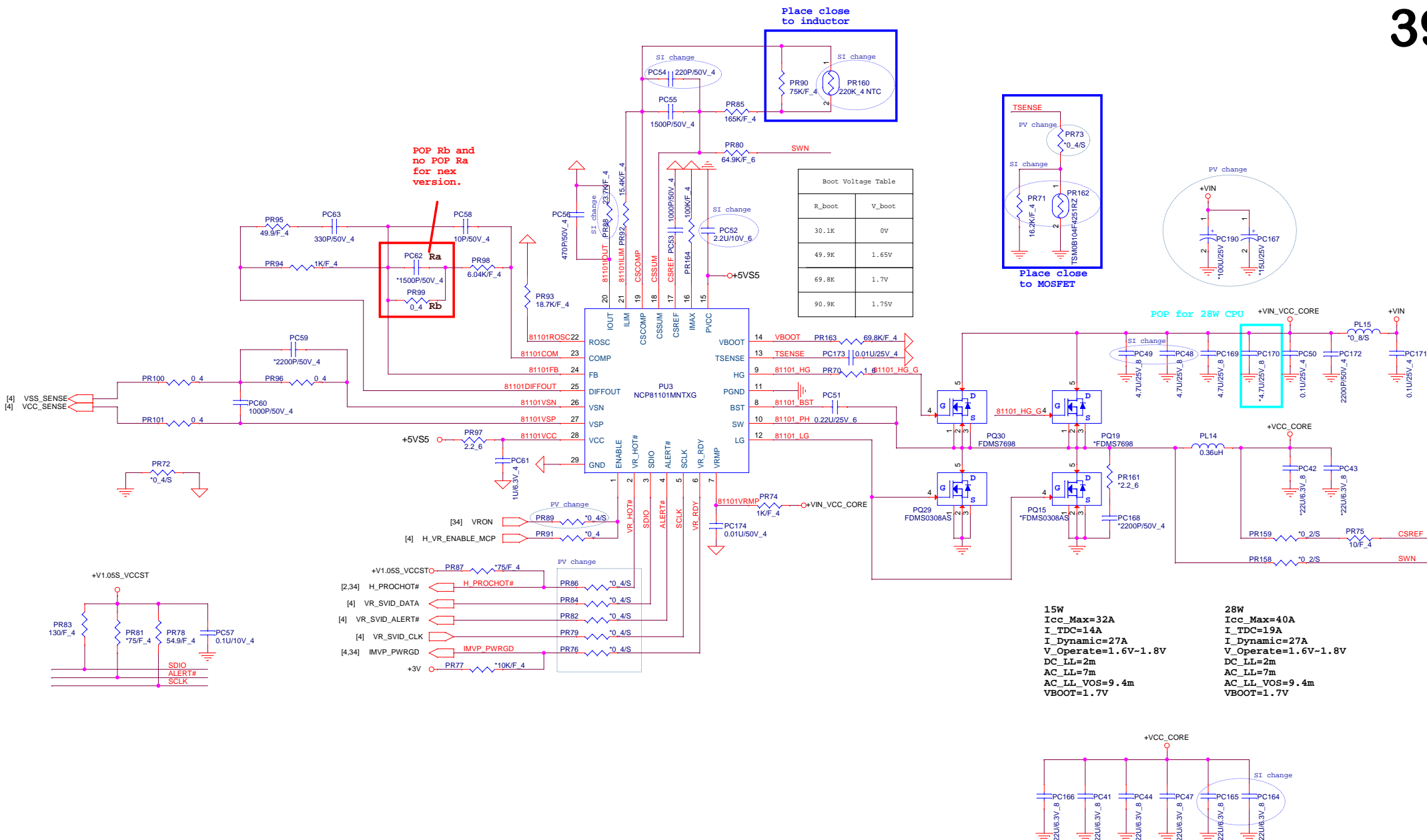
**PROJECT : Y02**  
**Quanta Computer Inc.**

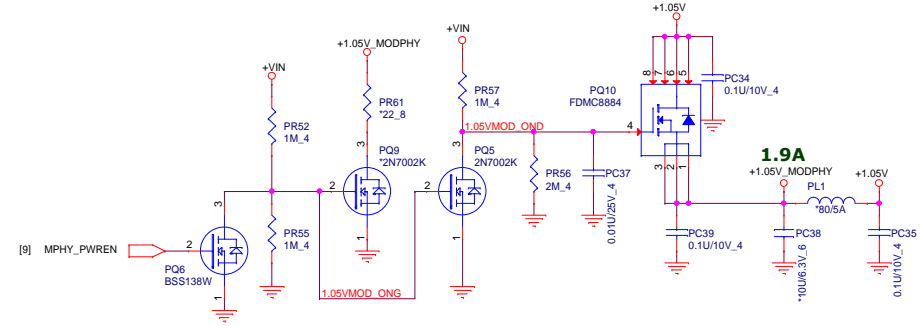
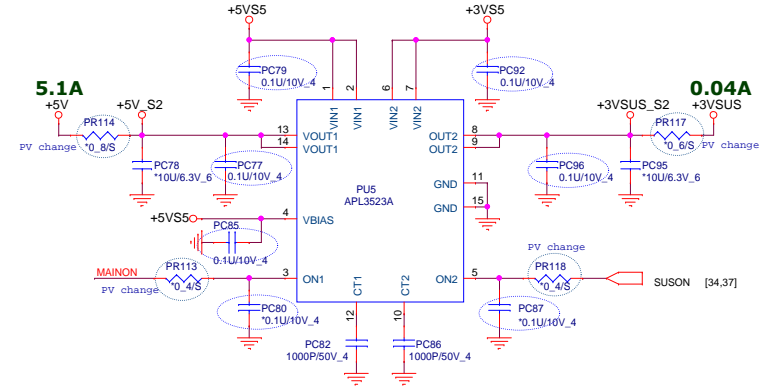
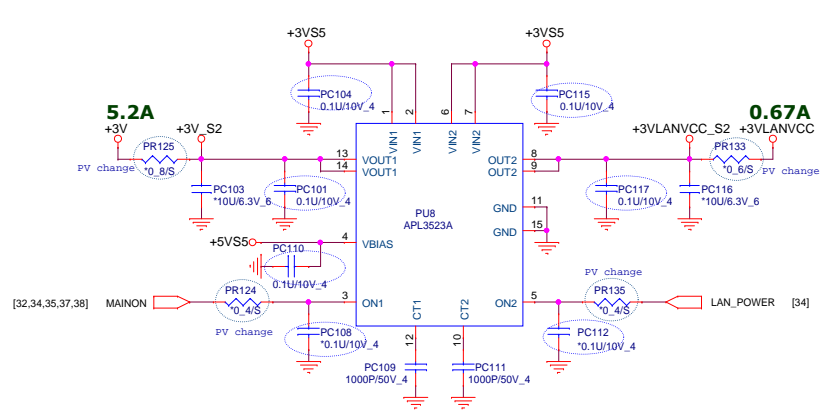
Size Custom	Document Number <b>DDR3 (RT8231A)/1.8V55</b>	Rev 1A
Date: Wednesday, April 02, 2014	Sheet 37 of 44	



+VIN [24,26,29,30,35,36,37,39,40,41,42,43]  
+3VS5 [6,7,9,10,11,25,29,32,33,36,40,43]  
+5VS5 [13,25,29,32,36,37,39,40,41,42,43]

 NB5/RD3	<b>PROJECT : U63</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number <b>+1.1VS5 (RT8228)/2.5V</b>	Rev 1A
	Date: Wednesday, April 02, 2014	Sheet 36	of 44

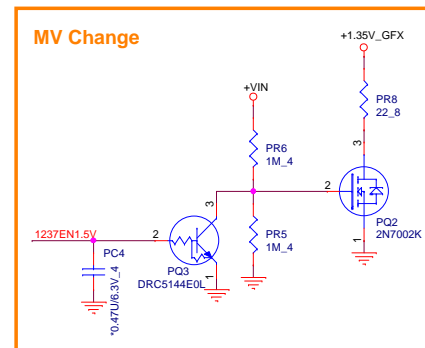
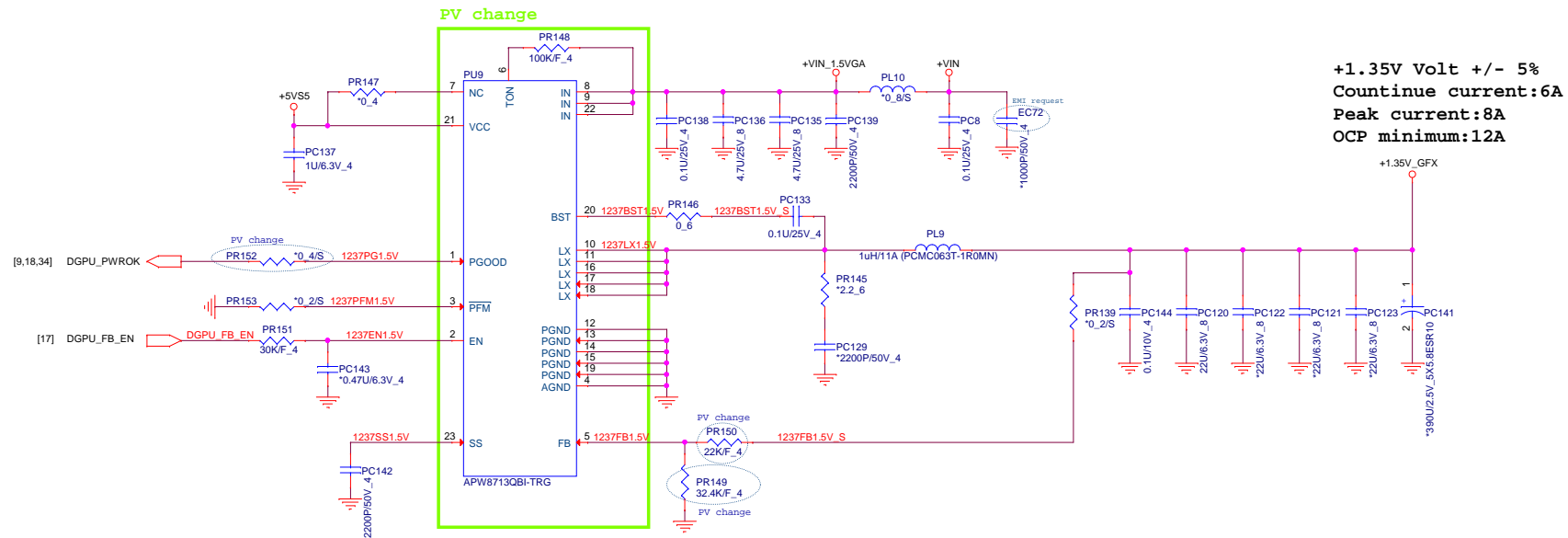


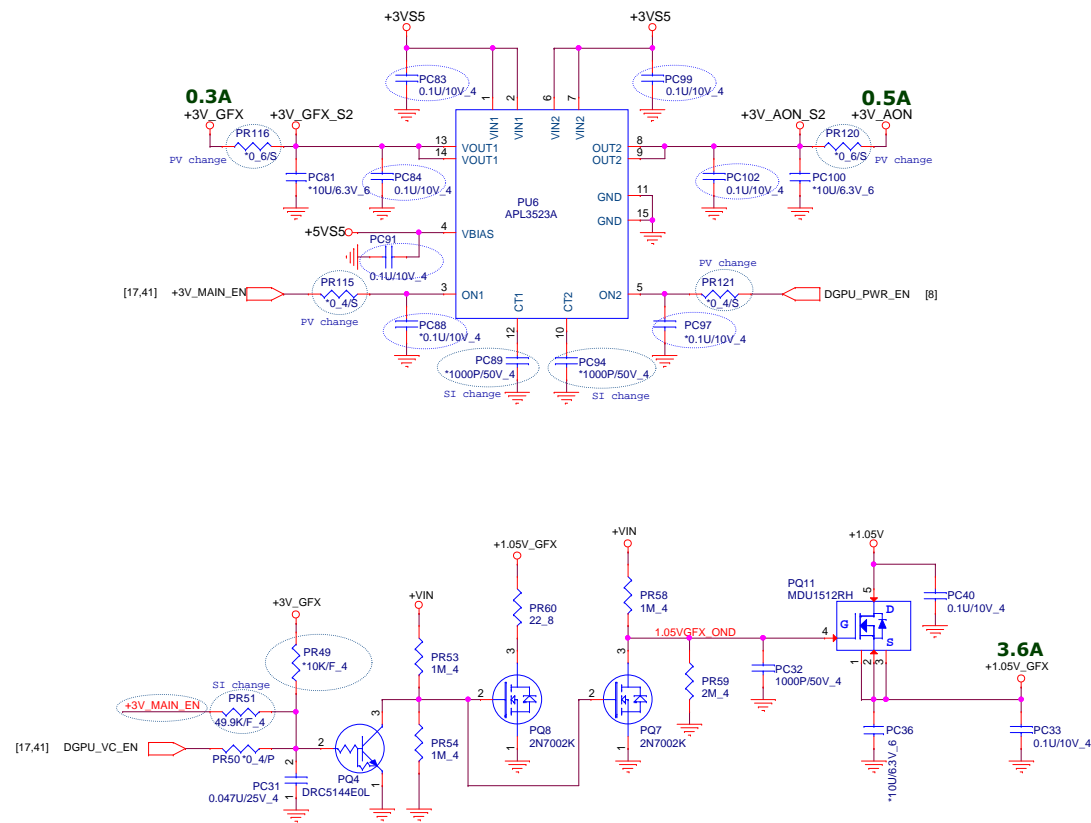



[6,7,8,9,10,11,12,13,14,17,18,23,24,25,26,27,28,29,30,31,33,34,39,41]	+3V
[24,25,26,29,30,31,32,33]	+5V
[24,26,29,30,35,36,37,38,39,41,42,43]	+VIN
[6,7,9,10,11,25,29,32,33,36,38,43]	+3VS5
[13,25,29,32,36,37,38,39,41,42,43]	+5VS5
[27,31]	+3VLANVCC

VGA TYPE	Ca, Cb
N15S-GX (25W)	No stuff
N15P-GT (35W)	Stuff







		<b>PROJECT :U83</b>	
		Quanta Computer Inc.	
Size Custom	Document Number 1.05V_VGA/3V_VGA	Rev 1A	
Date: Wednesday, April 02, 2014	Sheet 43	of 44	

Battery Connector	Pavillion	ENVY
14"	DFAD08MR063	DFAD08MR064
15"	DFAD08MR065	DFAD08MR066
17"	DFFC20FR081	DFFC20FR081

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41 、 42 、 43 ,but keep below location
Page 41	PC161 、 PC162
Page 42	PC138 、 PC144 、 PC4 、 PC148
Page 43	PC84 、 PC102 、 PC88 、 PC97 、 PC40 、 PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151 、 PC160	NA
	PQ21 、 PQ23 、 PQ25 、 PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151 、 PC160	Stuff
	PQ21 、 PQ23 、 PQ25 、 PQ28	Stuff

Title			
<Title>			
Size A	Document Number		Rev
	<Doc>		<RevCode>
Date:	Wednesday, April 02, 2014		Sheet 44 of 44